IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF WISCONSIN

SanDisk Corporation, Plaintiff, vs. Phison Electronics Corp., et al. Defendants.	)	Civil Action Nos.: 07-C-0605-C and 07-C-0607-C

SANDISK'S OPENING CLAIM CONSTRUCTION BRIEF

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TABLE OF ABBREVIATIONS

Smith Decl.	Decl. of Ryan R. Smith in Support of SanDisk's Opening Claim Construction Br.
'842 patent	U.S. Patent No. 6,757,842 B2 (Ex. 1 to Smith Decl.)
'316 patent	U.S. Patent No. 6,149,316 (Ex. 2 to Smith Decl.)
'808 patent	U.S. Patent No. 6,149,316 (Ex. 3 to Smith Decl.)
'893 patent	U.S. Patent No. 6,426,893 B1 (Ex. 4 to Smith Decl.)
'424 patent	U.S. Patent No. 6,763,424 (Ex. 5 to Smith Decl.)
'011 patent	U.S. Patent No. 7,137,011 B1
Intel Data Sheet	Intel 27F256 CMOS Flash Memory, data May 1988 (Ex. 6 to Smith Decl.)
Seeq Data Sheet	SEEQ 48F512 512k FLASH EEPROM, dated Oct. 1988 (Ex. 7 to Smith Decl.)
Yamagami patent	U.S. Patent No. 5,644,539 (Ex. 8 to Smith Decl.)
Oxford English Dictionary	The Oxford English Dictionary (2nd Ed. 1991) (excerpts attached as Ex. 9 to Smith Decl.)
Comm'n Op.	Comm'n Op. U.S. ITC Inv. 337-TA-619, dated Oct. 28, 2009 (excerpts attached as Ex. 10 to Smith Decl.)
'424 Prosecution History	Amendments and Response to Nov. 27, 2002 Office Action (dated Mar. 26, 2003) (Ex. 11 to Smith Decl.)
Computer Dictionary	Microsoft Press Computer Dictionary (2nd Ed. 1994) (excerpts attached as Ex. 12 to Smith Decl.)
Tuma patent	U.S. Patent No. 5,070,474 (Ex. 13 to Smith Decl.)
Taylor Decl.	Expert Declaration Of David L. Taylor, dated June 22, 2010
Robinson patent	U.S. Patent No. 4,746,998 (Ex. 2 to Taylor Decl.)

I. INTRODUCTION

The story of SanDisk began in 1988 with a man and his dream. The man was Dr. Eli Harari and his dream was to develop true portability for computer data. He believed that the way to achieve portability and a host of other benefits was through flash memory systems that would replace disk drives as the mass storage memory system of choice for computers. Today, the concepts Dr. Harari pioneered are literally assumed as commonplace, but at the time, conventional wisdom taught that flash memory was too expensive, too slow, and too unreliable. Fortunately, several other equally remarkable visionaries shared Dr. Harari's dream, including Sanjay Mehrotra, a co-founder of SanDisk, and Bob Norman, an early SanDisk employee.

The SanDisk story remains one of the most compelling and important stories of the modern computer age. SanDisk changed the way the world viewed and used mass storage. Indeed, Harari, Mehrotra and Norman's novel disk drive emulation system is described here in the patent application that issued as the '842, '316 and '808 patents. The industry has acknowledged these inventions as being fundamental. *See* Smith Decl. Ex. 16 (IEEE Johnson Award). Not surprisingly, SanDisk continued to innovate and the '011, '893 and '424 patents followed, as well, from the groundbreaking vision of the remarkable group that continued to believe that portability could be achieved and could be made affordable for all.

Of course, today we know that the computer and electronics industries, and the public throughout the world, eventually embraced SanDisk's flash memory system technology. Faced with true giants in computing with virtually unlimited capital and other resources, SanDisk needed not only spectacular technology protected by patents, but it needed a method as well to bring that technology to the market that would be embraced by the public and by those enormous competitors. So, SanDisk developed a unique approach that broadly licensed the inventions to the major companies in the flash memory industry. In recognition of the extraordinary novelty and adaptability of this new approach to mass storage, companies throughout the flash memory industry entered into license agreements with SanDisk.

A few companies—including defendants Kingston and Imation—have refused to appropriately license the SanDisk technology. Instead, they embarked on a pattern of infringement that has, for them, proven quite profitable. Kingston's founder and CEO (David Sun) is now a billionaire and listed by Forbes Magazine as one of the world's wealthiest. *See* Smith Decl. Ex. 17.

This litigation represents a critical moment in the protection of groundbreaking technology. While the issues before this Court will center around six particular patents, the ultimate outcome will have a far-reaching impact on innovation and the importance of entrepreneurship to development of yet unknown inventions.

Here, at the claim construction stage, the parties dispute the meaning of fifteen terms and phrases that appear in five of the six asserted patents. The defendants seek to contort the meaning of nearly every one of these terms and phases beyond recognition in an effort to escape a finding of infringement. To do so, they rely, repeatedly, on the same three tactics: (1) engaging in a wholesale rewrite of unambiguous claim language; (2) reading-in technical details from the specification as if those detail were themselves claim limitations; and (3) construing the claims so restrictively as to exclude even a preferred embodiment.

By way of example, claim 20 of the '424 patent explicitly recites the terms "***data***" and "***logical page addresses***" and consistently distinguishes between the two claim terms. The final step of claim 20 recites "***reading*** and assembling ***data*** from the first and second plurality of pages." The defendants' proposed construction is "***reading the logical page address*** within the first and second plurality of pages and thereafter assembling the data portions from the most up-to-date pages into a data file." In other words, the defendants improperly swap out the term "data" (which means one thing) for "logical page address" (which means something very different).

The defendants' clearly erroneous construction of the final step of claim 20 begs the question: On what basis could the defendants possibly have for proposing such a construction? The construction has no support in the language of the claims or the specification of the '424

patent. Instead of the intrinsic evidence, the defendants rely upon a non-precedential claim construction opinion from an Administrative Law Judge, which was *never tested* before the Federal Circuit.[1] Such an opinion is not a substitute for the intrinsic (and in a few cases extrinsic) evidence that the Federal Circuit requires courts to use to construe patent claims. The Court should reject the defendants' erroneous approach. It should, instead, adopt SanDisk's proposed constructions, which as explained herein, are firmly based on the rules promulgated by the Federal Circuit.

This brief first provides the Court with some background of the technology at issue in this case before turning to the five asserted patents for which the parties seek construction.[2]

II. TECHNOLOGY BACKGROUND

The asserted claims concern the management of flash memory for mass storage applications.[3]

A. Computer Systems

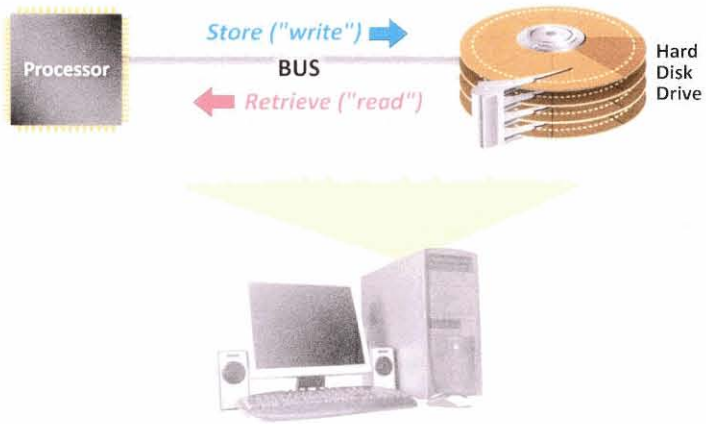
Computer systems, such as personal computers and notebooks, are seemingly everywhere in daily life. These systems are used for a host of purposes including email, word processing, and digital photographs. Though different, these applications all require the long-term storage of information (*e.g.*, digital photographs, scanned documents, Word files). For this, a computer has traditionally used disk storage, such as magnetic hard disk drives or floppy disk drives. These magnetic disk memories are relatively cheap; indeed, it is low enough in cost to store a vast library of information. Disk storage has the further advantage of being non-volatile—it can hold

[1] The lack of reliability of the ITC Administrative Law Judge construction was confirmed by the ITC itself, which rejects and/or modified several claim constructions. Comm'n Op. at 15.

[2] SanDisk and Imation have agreed to be bound by the constructions made in the ITC Investigation with respect to the '011 patent. Kingston is not accused to of infringing this patent.

[3] Flash memory is formally called "flash EEPROM"— flash electrically erasable programmable read-only memory. Computer Dictionary at 168.

the data even when the electrical power is turned off. The following diagram illustrates a hard disk drive connected to a computer's processor:



As shown, both the computer's processor and the hard disk drive reside inside the computer. The processor issues "write" commands to the hard disk drive and, at some later time, issues "read" command to retrieve that information. Popular operating systems such as Windows, Mac, Unix and Linux were specifically designed to operate with a hard disk drive for purposes of mass storage.

Despite having many advantages, magnetic disk memory systems had several limitations that hampered their ability to operate in mobile applications such as cellular telephones and digital cameras. For one, disk drive systems contain high-precision moving mechanical parts and, as a result, can "crash" when the read/write heads of the disk drive physically come in contact with the magnetic media. '842 patent at 1:22-25. Such crashes can irreparably corrupt the data on the magnetic disk. In addition, disk drives consume significant amounts of power. *Id.* at 1:25-26.

For years, companies (both big and small) tried but ultimately failed to create a semiconductor memory that overcame these problems. By way of example, some companies attempted to use DRAMs (Dynamic Random Access Memory) and SRAMs (Static Random Access Memory) to replace disk drives prior to the invention of the '842 and '316 patents. However, DRAMs and SRAMs were not viable options, in part because they are volatile memories (*i.e.*, they cannot retain data without constant power). '842 patent at 1:26-31.

Conventional wisdom taught that this shortcoming could be overcome with batteries and other redundant power supply systems to maintain the integrity of stored data. *See* Tuma patent at 14:58-60 ("A battery backup module is part of the solid state [DRAM] memory.").

B. Flash Memory

Flash memory is a form of semiconductor memory. It is fabricated by placing circuit patterns on a semiconductor wafer to form integrated circuit chips. Each flash memory integrated circuit chip includes an array of memory cells. These memory cells act as the storage media of the flash memory. A memory cell may include a "floating gate" that stores charge that is associated with digital data (*e.g.*, 0 or 1). Flash memory is a non-volatile memory because the storage element of the memory cell (*e.g.*, the floating gate) will retain the data even when power is removed from the memory device.

Using flash memory for mass storage applications (such as replacing a hard disk) presents several significant challenges. First, unlike magnetic disk memory, DRAM or SRAM, flash memory must be erased before it can be rewritten. This is complicated by the fact that flash memory cells cannot be erased individually. Rather, a large number of cells must be erased together at the same time. The computer industry coined the term "flash" from this requirement.[4]

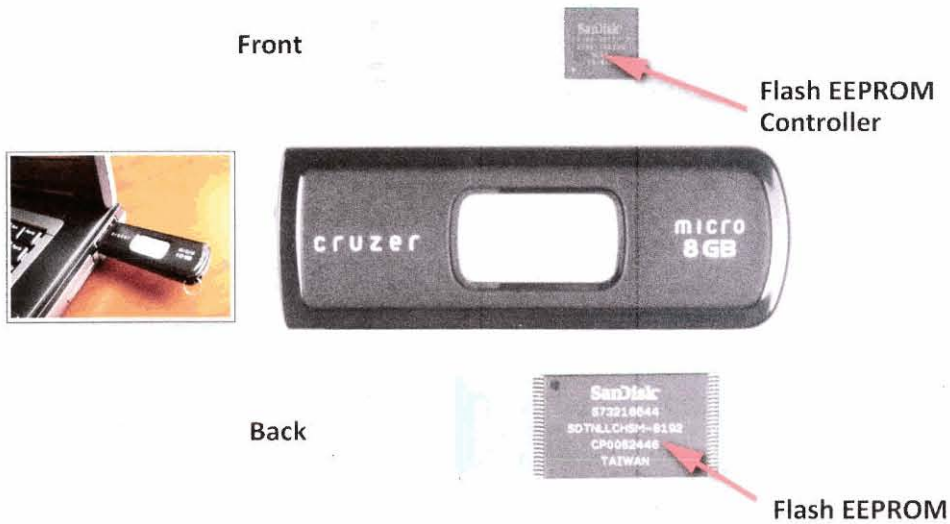
The second significant challenge to using flash memory for mass storage applications is the limited lifetime of flash. Provided they avoid a "crash" situation, the platter or disk of a hard drive can undergo millions of read/write cycles. Unfortunately, the process of writing and erasing data in flash will eventually destroy the memory cells. Each time a memory location is written or erased, the non-volatile floating gate storage element (and surrounding area) ages. As the cells age, they become increasingly likely to generate errors. For example, around the time when Dr. Harari founded SanDisk and filed the original application for many of the patents-in-

[4] The fact that a relatively large amount of memory is erased together distinguishes flash from EEprom memory, which typically erases at the byte or word level (*i.e.*, either 8 or 16 memory cells). That is, all the memory cells are erased together in a "flash."

suit, flash had a lifetime of between 100 and 1000 write/erase cycles. Intel Data Sheet at 1; Seeq Data Sheet at 1.

Because of its erase requirement and low endurance, flash was initially used for semi-permanent storage of data or program instructions that required only limited modification. Due, in large part, to the inventions at issue in the present action, SanDisk overcame these limitations and developed a flash based disk emulation system. Others followed.

Today, manufacturers use Flash memory in a variety of storage system. Perhaps most recognizable are USB flash drives, like the one illustrated below:



As shown above, a USB flash drive attaches to a computer's USB port and allows users to read and write data to carry to other computers. These flash drives typically contain one or more flash chips (often together in a rectangular black package) and a flash controller. This controller acts as the memory system's "brain." It accepts commands from the host system (such as the notebook computer pictured above) and, based on those commands, either writes data to, or retrieves data from, the accompanying flash memory chips. Because the computer's operating system expects to see a hard disk drive, the controller must accept the same commands provided to a hard disk drive. However, as explained above, there are major differences between flash and hard disk drive memory, which makes dealing with these commands a challenge to say the least.

III. LEGAL STANDARDS

A. Claim Construction

The claims of a patent define the scope of the invention. *See Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 373 (1996). The interpretation of claim language is a question of law for the Court to decide. *Id.* at 391. It is not, however, "an obligatory exercise in redundancy." *U.S. Surgical Corp. v. Ethicon, Inc.*, 103 F.3d 1554, 1568 (Fed. Cir. 1997). That is, a district court need not repeat or restate claim language unless necessary for "resolution of disputed meanings and technical scope, to clarify and when necessary to explain what the patentee covered by the claims." *Id.*

In interpreting the claims, the Court should primarily look to intrinsic evidence, which includes the claim language, the specification, and the prosecution history. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-17 (Fed. Cir. 2005). While dictionary definitions serve a useful purpose in ascertaining the meaning of words, "in those circumstances where reference to dictionaries is appropriate, the task is to scrutinize the intrinsic evidence in order to determine the most appropriate definition." *Free Motion Fitness, Inc. v. Cybex Int'l, Inc.*, 423 F.3d 1343, 1349 (Fed. Cir. 2005).

The words of a claim are to be given their ordinary and customary meanings. *See Phillips*, 415 F.3d at 1312. When a technical term is used in a claim, the meaning of the term is the technical meaning that would have been used by one of ordinary skill in the art. *See Atofina v. Great Lakes Chemical Corp.*, 441 F.3d 991, 996 (Fed. Cir. 2006). But "in some cases, the ordinary meaning of claim language as understood by a person of skill in the art may be readily apparent even to lay judges, and claim construction in such cases involves little more than the application of widely accepted meaning of commonly understood words." *Phillips*, 425 F.3d at 1314.

The claim terms also are to be construed in the context of the entire patent, including the specification. *See Phillips*, 415 F.3d at 1313. The specification "is always highly relevant to the claim construction analysis." *Id.* at 1315. The Federal Circuit has, however, "cautioned against

reading limitations into a claim from the preferred embodiment described in the specification, even if it is the only embodiment described, absent clear disclaimer in the specification." *In re American Academy of Science Tech Center,* 367 F.3d 1359, 1369 (Fed. Cir. 2004).

Finally, the Court must consider the prosecution history. Because the prosecution history contains the complete record of all the proceedings before the Patent Office, including representations made by the applicant regarding the scope of the claims, it "is often of critical significance in determining the meaning of the claims." *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996).

The prosecution history includes the prior art cited during the examination of the patent. *See Phillips*, 415 F.3d at 1317. Thus, "prior art cited in a patent or cited in the prosecution history of the patent constitutes intrinsic evidence." *Kumar v. Ovonic Battery Co., Inc.*, 351 F.3d 1364, 1368 (Fed. Cir. 2003).

B. SanDisk's Proposal for the Definition of One of Ordinary Skill in the Art Should be Adopted

The '842, '316, '808, '893, and '424 patents for which the parties seek construction relate to memory devices that use flash memories. In this field of art, a person of ordinary skill would have had (i) a minimum of Bachelor of Science degree in Electrical Engineering or equivalent professional experience and (ii) one-to-two years of experience in the design of non-volatile semiconductor memories and/or the design of systems incorporating non-volatile semiconductor memories. Taylor Decl. ¶ 20.

SanDisk's proposal is consistent with the factors relevant to determining the level of ordinary skill in the art. *See Envtl. Designs Ltd. V. Union Oil Co.*, 713 F.3d 693, 696 (Fed. Cir. 1983). As stated in the declaration of Mr. Taylor (a longtime expert in this field), the types of problems encountered in this art and the sophistication of the technology are both within the scope of a bachelor's degree in electrical engineering when coupled with one-to-two years of experience. Taylor Decl. ¶ 20. Moreover, this was a rapidly evolving art in which active workers in the field depended on experience more than extensive formal education.

SanDisk's proposal is also consistent with other cases involving similar fields of art. *See, e.g.*, *DePaul v. Toshiba Corp.*, 1995 U.S. Dist. LEXIS 11688, at *27 (S.D.N.Y. 1995) (stating that "a person of ordinary skill in the art of memory board designing would be one either with no degree but with three or four years of experience, or one with a bachelor's degree in electrical engineering and one or two years of experience"). Thus, SanDisk's proposed level of skill is correct.

C. The Prior ITC Claim Construction is Irrelevant to Claim Construction in this Case

Two of the patents at issue (the '424 and '893 patents) were the subject of a prior claim construction opinion issued by an administrate law judge of the U.S. International Trade Commission ("ITC"). That opinion is not germane to claim construction in this case. *Bio-Technology General Corp. v. Genentech, Inc.*, 80 F.3d 1553, 1564 (Fed. Cir. 1996); *see also Texas Instruments, Inc. v. United States Int'l Trade Comm'n*, 851 F.2d 342, 344 (Fed. Cir. 1988) ("this court has stated that the ITC's determinations regarding patent issues should be given no res judicata or collateral estoppel effect."). Simply put, the Court should not rely on the ITC's determination as a substitute for the hierarchy of claim construction evidence outlined above.

IV. SANDISK'S PROPOSED CONSTRUCTIONS SHOULD BE ADOPTED BY THE COURT

A. The Flash EEPROM System Patents

The '842, '316, and '808 patents all stem from the same original patent application filed by inventors Eli Harari, Sanjay Mehrotra, and Bob Norman and are collectively referred to herein as the "Flash EEPROM System" patents, which is the title that they share. In general terms, the '842 and '316 relate to the flash based disk emulation system while the '808 patent relates to multi-sector erase techniques for such a system. This section first provides a brief overview of these patents (the '842 and '316 patents are addressed together because their

inventions are similar) before turning to the seven claim terms from these patents that are in dispute.

1. Overview of Flash EEPROM Patents

a. The '842 and '316 Patents

The patented inventions are directed to an innovative memory system on a card that communicates with a computer system in the same manner as a disk drive. '842 patent at 7:58-62. This computer system is illustrated in the following figure from the patents:

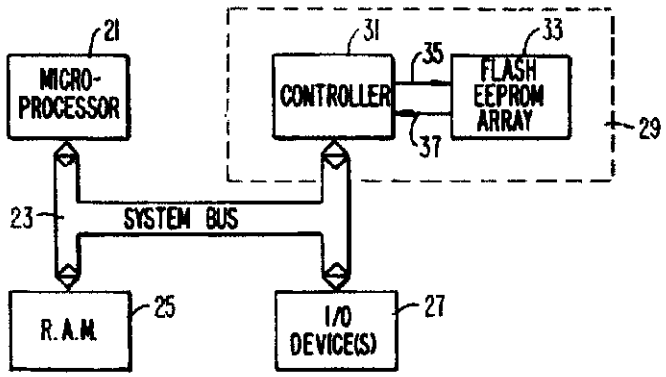


FIG._1A.

This figure shows that the memory system (noted by the dashed-line) includes a controller and one or more flash integrated circuit chips. '842 patent at 3:56-58. This memory system is connected to the computer's system bus (the host) which, like the USB flash drive depicted in the Technology Background section, communicates with the computer's microprocessor, RAM, or input / output devices. Among other duties, the controller receives read and write commands along with user data from the host computer in the same addressing format used by magnetic disk drives.

In this context, "user data" generally refers to the data that the host system wishes to store in, or read from, the memory card such as a digital picture or word processing document. The memory controller, within the memory card, translates these commands from the hard disk

addressing format into a flash addressing format. Then, in the case of a write, the memory controller commands the flash memory to store the user data along with overhead data.

This "overhead" data—which typically includes error correction codes ("ECC"), addressing information, and other data generated within the memory card—is crucial to surmounting the inherent limitations of Flash memory. For instance, ECC detects and corrects data errors that occurred during the storage of data in memory. '842 patent at 8:10-14. ECC, therefore, greatly enhanced the reliability and endurance of flash memory systems. *Id.* at 8:18-21.

This was a strange notion in 1988. Indeed, Hitachi, then one of the leaders in flash memory technology, believed that "flash memory need not have any ECC … because the error rate thereof is much lower than that of the magnetic disk storage device." *See* Yamagmi at 11:44-47.

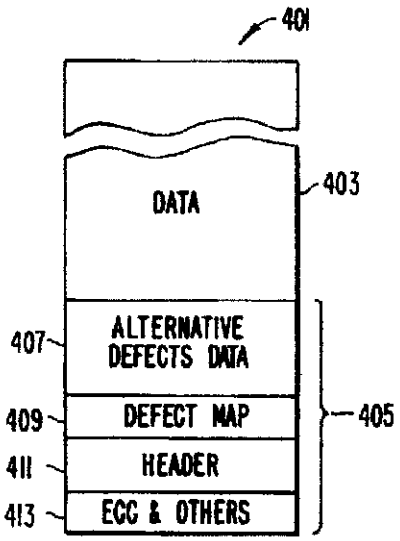
The inventors did not stop there. They realized that, to further overcome the inherent limitations of flash, the overhead data must be stored in the same block (or sector) as the corresponding user data. But this was easier said than done.

When Dr. Harari and his co-inventors conceived of the inventions, flash memory was either chip erasable (meaning that all the memory cells within the array were erased in one "flash") or block erasable (where a portion of the array equal to one or more units of data is erased at once). The chip erasable flash was ill suited for computer systems which would typically read (and write) in 512-byte units, as opposed to the entire memory at once. '842 patent at 4:56-63.[5] Thus, to change even one 512-byte unit, the contents of the entire memory would have to be read out of the device, maintained in another memory, and reprogrammed into the device (along with any update date) following the erase operation. *Id.*

[5] An example of a chip erase device is the Intel flash device discussed at column 4, lines 41-50 of the '842 Patent. Intel Data Sheet at 8-9. As shown in its data sheet, the Intel flash erases 32768 bytes of data (*i.e.*, 32768 x 8 memory cells) in a single erase operation.

The block erasable flash then available to the inventors was better (in that it allowed for the modification of individual 512-byte units) but was designed in a manner that did not contemplate storing user data and overhead data in the same erasable block. '842 patent at 4:56-64.[6] Thus, to store a single 512-byte unit the controller would require at least two erase blocks: one for the user data and another for the overhead information.

To overcome this problem, the inventors had to redesign flash memory to include room for both user data and overhead data within the same erasable block. When paired with such a flash memory, the controller may erase "old" or "invalid" user and overhead data in a single erase operation. This redesigned block is shown in Figure 5 of the patent, which is reproduced below:



SECTOR PARTITION

FIG. 5.

As shown above in Figure 5, the ECC and other overhead data are stored within the same block as the user data. A defect map may also be included as part of the overhead data stored in

[6] An example of a block (or sector) erase device is the Seeq flash device discussed at column 4, lines 51-58 of the '842 Patent. As shown in its data sheet, the Seeq flash erases 512 bytes (*i.e.*, 512 x 8 memory cells) in a single erase operation.

the same sector as the user data. Like ECC, this map increases the endurance of a memory sector.

The "Header" portion of the overhead data is used to store the mass storage memory address from the host. '842 patent at 9:11-13. Recall, that because invention emulates a hard disk, the computer system provides addresses just as it would address a hard disk drive. As discussed in the Technology Background section, a typical way to address hard disk in the late 1980s was with the "cylinder, head, sector" format.[7] Even though flash memory does not have "cylinders" or "heads," the controller described in the patents translates these types of disk addresses into a block/sector addresses within the flash memory.[8] Taylor Decl. at ¶ 11. These addresses are stored as part of the overhead data to ensure that the association is maintained. '842 patent at 9:17-34.

In one embodiment of the '842/'316 patents, the controller identifies and stores addresses of defective sectors within the flash memory array to prevent further use of the defective sector. '842 patent at 11:48-51. As the patent explains, "[w]hen the controller is given an address to access data, the controller compares this address against the sector defect map. If a match occurs then access to, the defective sector is denied and the substitute address presenting the defect map is entered, and the corresponding substitute sector is accessed instead. '842 patent 11:62-65. This substitution technique significantly increases the useful life of the memory system, because the failure of one block does not spell doom for the entire memory system.

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[7] In the late 1980s, another common, well-known addressing format for magnetic disk sectors was the LBA (or logical block address). Taylor Decl. at ¶ 9. This common addressing format is illustrated in, for example the Robinson patent, which is cited reference and thus part of the intrinsic record. As discussed below, the claims of the '842/'316 patents are not limited to any particular format of hard disk addressing.

[8] A magnetic disk "sector" was typically 512-bytes and was the unit of both read and write in a disk drive. A flash memory "sector" was a unit of erase. A flash memory sector (also called a block) could store one or more disk sectors of data.

Through these, and other novel techniques, the '842 and '316 patents overcame the inherent limitations of flash and re-introduced it as a viable alternative to hard disk memory.

b. Overview of the '808 Patent

As explained above, some conventional flash memories were "chip" erase while others were "block" erasable. Not only did these architectures lack room to store overhead with the user data, they also proved too slow for hard disk emulation applications. In particular, to update some (but not all) of the data in a chip erase memory required reading out the unchanged data, storing it, erasing the entire chip, and then reprogramming the chip with the new data and the unchanged data. '808 patent at 4:33-42. The block erase flash memory was slow for a different reason. Namely, the blocks had to be erased one-by-one. *Id.* at 4:43-50. This could take a long time, especially if there was lots of data to update.

The '808 patent represents an important improvement to the sectored / block erasable flash memory systems. The patent explains that "[e]ach sector can be addressed separately and selected for erase," and the system can select different combinations of these sectors for erase. '808 patent at 4:67-5:1. This is illustrated in the following figure:

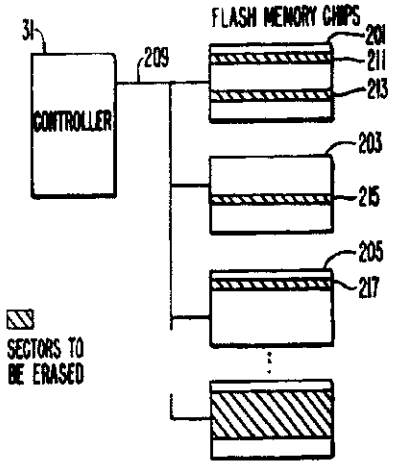

FIG._2.

The above figure depicts a memory system with a controller and several flash memory chips. In this example, the controller selects two sectors to erase from the first chip (labeled 201)

and a single sector from both the second chip (labeled 203) and the third chip (labeled 205). The controller also selects numerous sectors from the bottom-most flash memory chip depicted. The patent explains that "[t]he sectors that were selected will all be erased together. This capability will allow the memory and system of the present invention to operate much faster than the prior art architecture." '808 patent at 5:5-8.

The inventors' multi-block erase architecture greatly enhanced system throughput, thus helping to put flash memory on par with the hard disk technology that it sought to replace.

2. The Disputed Claim Terms

The claims in which the disputed terms of the Flash EEPROM System patents appear are listed below. The disputed terms are in bold:

> ['842 patent] 1. A method of operating a memory system with a host system, wherein the memory system includes an array of non-volatile memory cells on an integrated circuit memory chip that is partitioned into a plurality of blocks that individually include a distinct group of memory cells that are erasable together as a unit, comprising:
>
> utilizing said memory chip and a memory controller within a card that is removably connectable to the host system, said controller being connectable to the host system for controlling operation of the memory system when the card is connected thereto,
>
> **operating individual blocks of memory cells with non-overlapping portions thereof storing at least user data and overhead information,**
>
> detecting a predefined condition when individual blocks become unusable and **linking the addresses of such unusable blocks with addresses of other blocks that are useable,**
>
> causing the controller, in response to receipt from the host system of **an address in a format designating at least one mass memory storage block,** to generate an address of a non-volatile memory block that corresponds to said at least one mass memory storage block,
>
> accessing a usable block of the memory system, if the block with the generated address is unusable, by referring to the linked address of another block that is usable and then accessing that other block,
>
> either writing data to, or reading data from, the user data portion of the accessed usable block, and
>
> either writing to, or reading from, said overhead portion of the accessed usable block, information related to either the accessed usable block or data stored in the user data portion of said accessed useful block.

['842 patent] 10. A method of operating a memory system with a host system, wherein the memory system includes an array of non-volatile memory cells on an integrated circuit memory chip that is partitioned into a plurality of blocks that individually include a distinct group of memory cells that are erasable together as a unit, comprising:

utilizing said memory chip and a memory controller within a card that is removably connectable to the host system, said controller being connectable to the host system for controlling operation of the memory system when the card is connected thereto,

operating individual blocks of memory cells with non-overlapping portions thereof storing at least user data and overhead information,

causing the controller, in response to receipt from the host system of **an address in a format designating at least one mass memory storage block**, to designate an address of at least one non-volatile memory block that corresponds with said at least one mass memory storage block,

either writing user data to, or reading user data from, the user data portion of said at least one non-volatile memory block, and

either writing to, or reading from, said overhead portion of said at least one non-volatile memory block, overhead data related either to said at least one non-volatile memory block or to data stored in the user data portion of said at least one non-volatile memory block.

['842 patent] 12. The method of claim 10, wherein the overhead data stored in said overhead portion of the individual blocks includes **addresses of the individual blocks**.

['842 patent] 61. A method of operating a memory system with a host system that includes a processor, wherein the memory system includes one or more integrated circuit chips individually including an array of non-volatile floating gate memory cells partitioned into a plurality of **sectors** that individually include a distinct group of memory cells that are erasable together as a unit, comprising:

providing said one or more of the memory integrated circuit chips and a memory controller within a card that is removably connectable to the host system, said controller being connectable to said processor for controlling operation of the memory system when the card is connected to the host system,

operating memory cells within individual **sectors** with at least a user data portion and an overhead portion,

causing the controller, in response to receipt from the processor of **an address in a format designating at least one mass memory storage block**, to designate an address of at least one non-volatile memory **sector** that corresponds with said at least one mass memory storage block,

either writing user data to, or reading from, the user data portion of said at least one non-volatile memory **sector**, and

either writing to, or reading from, said overhead portion of said at least one non-volatile memory **sector**, overhead data related either to said at least one non-volatile memory sector or to data stored in the user data portion of said at least one non-volatile memory **sector**.

['842 patent] 63. The method of claim 61, wherein the overhead data stored in said overhead portion of the individual **sectors** includes **addresses of the individual sectors**.

['316 patent] 67. A method of operating a memory system with a host system that includes a processor, wherein the memory system includes one or more integrated circuit chips individually including an array of non-volatile floating gate memory cells partitioned into a plurality of **sectors** that individually include a distinct group of memory cells that are erasable together as a unit, comprising:

providing said one or more chips and a memory controller within a card that is removably connectable to the host system, said controller being connectable to said processor for controlling operation of the memory system when the card is connected to the host system,

operating the memory cells within the individual **sectors** with at least a user data portion and an overhead portion,

causing the controller, in response to receipt from the processor of **an address in a format designating at least one mass memory storage block**, to designate an address of at least one non-volatile memory **sector** that corresponds with said at least one mass memory storage block,

either writing user data to, or reading from, the user data portion of said at least one non-volatile memory **sector**, and

either writing to, or reading from, said overhead portion of said at least one non-volatile memory **sector**, overhead data related either to said at least one non-volatile memory **sector** or to data stored in the user data portion of said at least one non-volatile memory **sector**.

['316 patent] 69. The method of claim 67, wherein the overhead data stored in said overhead portion of the individual **sectors** includes **addresses of the individual sectors**.

['316 patent] 79. A memory system connectable to a host processor to enable the exchange of data therebetween, and memory system comprising:

an array of non-volatile floating gate memory cells partitioned into a plurality of blocks of cells that individually store a given amount of user data and overhead data, wherein the memory cells are individually programmable into one of more than two distinct threshold level ranges corresponding to more than one bit of data per cell, and

a controller connected to the array and removably connectable to the host through an electrical connector, said controller including:

an address generator that is responsive to receipt of a **mass memory storage block address** from the host to address a corresponding at least one of the plurality of memory blocks, and

a data transfer control that responds to an instruction from the host to perform a designated one of reading user data from, or writing user data to, said at least one address block, including a data writing circuit that generates at least some of the overhead data associated with at least one of at least one addressed block or user data being written therein, and a data reading circuit that reads the overhead data from said at least one addressed block, wherein the data writing circuit programs the individual memory cells into said one of more than two distinct threshold level ranges and the data reading circuit reads one of more than two distinct threshold level ranges from the individual memory cells.

['808 patent] 16. A method of operating a memory system having an array of EEPROM cells divided into multiple non-overlapping **sectors** that individually contain a plurality of said cells sufficient to store multiple bytes of data and which are erasable together, comprising:

(a) designating a combinations of a plurality of but less than all of said multiple **sectors** to be erased,

(b) erasing the combination of **sectors** without erasing others of said multiple **sectors**,

(c) after the combination of **sectors** has been erased, writing data in at least some of the erased combination of **sectors**, and

(d) repeating the operations of (a) through (c) with another combinations of **sectors**.

3. SanDisk's Constructions for the Flash EEPROM System Patents Should Be Adopted

a. "sector"

SanDisk's Proposed Construction	Defendants' Proposed Construction
The basic unit of erase of the flash memory cell array on an integrated circuit chip. To further clarify: A "sector" is smaller than the array. Each array contains two or more sectors. A "sector" is larger than the unit of erase for an EEprom (*e.g.*, a byte or word)	the basic unit of erase

The term "sector" appears in asserted claims 61 of the '842 patent, claim 67 of the '316 patent, and claim 16 of the '808 patent. The parties agree that this term should be construed the same way for each of these claims. The parties further agree that a sector is a basic unit of erase.

Where the parties disagree is whether the term "sector" refers to basic unit of erase in a flash memory chip as taught by the Flash EEPROM System patents or whether the term "sector" can refer to ***any*** basic unit of erase as claimed by defendants.

Both the plain language of the claims and the specification compels SanDisk's proposed construction. As to the claims, they show that the term "sector" has the required attributes for the basic unit of erase in a flash memory device. Namely, the "sector" is (1) a partition of the memory array and (2) sector is comprised of a substantial number of memory cells. For example, the preamble of claim 61 of the '842 patent recites a "memory system" with "one or more integrated circuit chips individually including an array of non-volatile floating gate memory cells partitioned into plurality of sectors that are erasable together as a unit."[9] '842 patent at 22:52-57.[10] *See Phillips*, 415 F.3d at 1314 ("the context in which a term is used in the asserted claim can be highly instructive."). Thus, the claim language confirms that a "sector" is a sub-division of an array of memory cells located on an integrated circuit chip (as opposed to, for instance, memory cells from different arrays).

Each array has two or more sectors. '842 patent at 22:51-57 ("an array of non-volatile floating gate memory cells partitioned into a plurality of sectors"). The language of claim 16 of the '808 patent further confirms that a sector is comprised of a substantial number of memory cells. Claim 16 defines a sector as "individually contain[ing] a plurality of said cells ***sufficient to store multiple bytes of data*** and which are erasable together." '808 patent at 17:27-28 (emphasis added). Likewise, the claims of the '842 and '316 patents recite operating "memory

[9] Claim 67 of the '316 patent includes preamble language substantially the same as claim 61 of the '842 patent. *See* '316 patent at 21:27-33.

[10] The Flash EEPROM System patents share the same specification. As a result, for the convenience of the Court, except when reciting specific claim language, this brief (where possible) will make citations to the specification of the '842 patent. The same figures and text can be found in the '316 and '808 patents.

cells within individual sectors with ***at least*** a user data portion and an overhead portion." '842 patent at 22:64-65 (emphasis added).

Thus, from the plain language of the claims, it is clear that (1) a sector is a basic unit of erase of an array on an integrated circuit chip; (2) that a "sector" is a sub-division and is smaller than the array and (3) a sector includes, at the very least, enough memory cells to store multiple bytes of data. Each of these three attributes confirms that the term "sector" refers to the basic unit of erase in a flash EEprom.

The specification also makes clear that a "sector" is the basic unit of erase in flash memory—as opposed to some other form of semiconductor. The patent is entitled "***Flash*** EEPROM System." '808 patent at [54]. The summary of the invention states that "an array of ***Flash*** EEprom cells on a chip ***is organized into sectors*** such that all cells within each sector are erasable at once." '842 patent at 2:1-3 (emphasis added). The specification further declares:

> In the present invention, the **Flash EEprom memory is divided into sectors** where all the cells within each sector are erasable together. Each sector can be addressed separately and selected for erase.

'842 Patent at 4:55-58 (emphasis added).

Finally, in the context of the invention, the patent goes on to state that "[t]he memory in each ***Flash*** EEprom chip is ***partitioned into sectors*** where all memory cells within a sector are erasable together. For example, each sector may have 512 byte (i.e. 512x8 cells) available to the user, and a chip may have 1024 sectors." *Id.* 5:5-8 (emphasis added). Indeed, every reference in the patent to an erasable "sector," is with respect to flash memory.

To leave-out the term "flash" from the definition of "sector" would run afoul of the Federal Circuit's requirement that claim language be interpreted in light of the "fundamental purpose and significance of the invention." *Minnesota Mining & Mfg. Co. v. Johnson & Johnson Orthopedics, Inc.,* 976 F.2d 1559, 1566-67 (Fed Cir. 1992), and in a manner "consistent with the further[ing] and purpose of the invention." *CVI/Betat Ventures, Inc. v. TuraLP*, 112 F.3d 1146, 1160 (Fed, Cir. 1997). Of the seven objects of the invention, ***all*** involve enhancing

some aspect of a "Flash EEPROM System" – as opposed to some other semiconductor system. '842 patent 1:42-62. And as explained above, the specification consistently refers to a "sector" as a basic unit of erase for a flash memory array.

In light of the intrinsic record, the Court should construe the term "sector" as "the basic unit of erase of the flash memory cell array on an integrated circuit chip."

b. "operating individual blocks of memory cells with non-overlapping portions thereof storing at least user data and overhead information"

SanDisk's Proposed Construction	Defendants' Proposed Construction
operating multiple erase blocks in the claimed memory system in a manner that stores both user data and overhead information in non-overlapping regions of the individual erase blocks. A block is not limited to only one user data portion and only one overhead data portion	operating one or more erase blocks in the claimed memory system in a manner that stores both user data and overhead information in non-overlapping regions of the individual erase blocks

This term appears in claims 1 and 10 of the '842 patent. The parties' dispute centers primarily on two issues: (1) whether the claimed methods can be performed by a system using a single block and (2) whether the claimed block is limited to a single user data portion and a single overhead portion.

The plain language of the claims resolves the first issue. The plain language recites "operating individual block**s**." '842 patent at 16:24-26 (claim 1), 17:31-33 (claim 10) (emphasis added). The use of the plural indicates the inventors' intent to require multiple blocks. This is reinforced by the inventors' choice of words in subsequent method steps. That is, to "designate an address of ***at least one*** non-volatile memory blocks" and either writing user data to, or reading user data from "***at least one*** non-volatile memory blocks." '842 patent at 16:32-36 (claim 1), 17:35-40. Had the inventors intended the disputed claim term to cover a single block, they would have drafted the claim as "operating ***at least one*** erase block …" because that is what the inventors consistently did to convey that a limitation could be met with a single block.

The defendants' "one or more" construction breaks-down even under the fiction that "block**s**" (in a vacuum divorced from the claim language) covers a single block. To be specific,

claim 1 recites "detecting a predefined condition when ***individual blocks*** become unusable and linking the addresses of such unusable blocks with addresses of ***other blocks*** that are usable. '842 patent at 16:27-31 (emphasis added). By definition, a memory system operating a single block could not perform "linking." Indeed, by operating only one block, there would be no block to which the unusable block could be linked.

"When the parties present a fundamental dispute regarding the scope of a claim term, it is the court's duty to resolve it." *O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1362 (Fed. Cir. 2008). Here, the fundamental dispute is whether or not "a block" of user data must have "*only one* user data portion and *only one* overhead data portion." The defendants seek to impose this "only one" limitation in order to create a non-infringement argument. This argument fails for several reasons.

First, nothing in the claim suggests such a limitation. Rather, the claims with the term at issue utilize the transitional phrase "comprising" which specifically allows additional elements. *See Gillette Co. v. Energizer Holdings, Inc.*, 405 F.3d 1367, 1371 (Fed. Cir. 2005) (holding that a claim for a razor "comprising a … a group of first , second, and third blades did not exclude a razor having four blades noting that the "word 'comprising' transitioning from the preamble to the body signals that the entire claim is presumptively open-ended").

Second, the defendants' "only one" limitation violates the doctrine of claim differentiation. In particular, claim 16 requires that the "individual blocks include ***only one user data portion*** and ***only one overhead data portion***." '842 patent at 18:7-9 (emphasis added). But that is precisely the limitation that the defendants impermissibly seek to read into claim 10. *See Seachange Int'l, Inc. v. C-COR Inc.*, 413 F.3d 1361, 1368 (Fed. Cir. 2005); *Envtl. Designs, Ltd. v. Union Oil Co.*, 713 F.2d at 699 (noting it would be "improper for courts to read into an independent claim a limitation explicitly set forth in another claim"), *cert. denied*, 464 U.S. 1043 (1984).

The Court should adopt SanDisk's proposed construction for the foregoing reasons.

c. "linking the address of such unusable blocks with addresses of other block that are usable"

SanDisk's Proposed Construction	Defendants' Proposed Construction
substituting the physical address of an unusable block with the physical address of a block that is usable	maintaining a map or table which includes the physical addresses of unusable blocks and the physical addresses of corresponding substitute blocks which are useable

The disputed term is found in claim 1 of the '842 patent. The parties agree that the "linking" step relates to replacing physical addresses of unusable blocks with physical addresses of blocks that are usable. The dispute concerns whether the claim term relates to substituting addresses, or whether it is limited to maintaining a correspondence table with the specific parameters identified in the defendants' proposed construction. When viewed in the context of the surrounding claim language, and in light of the specification, "linking" refers to "substituting" and is not limited to maintaining this specific table.

The disputed claim term appears in the element of claim 1 of the '842 patent in the following context:

> detecting a predefined condition when individual blocks become unusable and linking the addresses of such unusable blocks with addresses of other blocks that are usable.

'842 patent at 16:28-31. Thus, in the context of claim 1, the disputed "linking" step pertains to circumstances in which the controller receives, from the computer system, an address that corresponds to an unusable (*e.g.*, defective) non-volatile memory block and links (substitutes) an address that corresponds to a block that is useable.

The other steps in the claimed method further inform the meaning of the disputed term. In particular, the fifth step of claim 1 states that when the claimed controller designates an unusable block, the memory system responds "by ***referring to the linked address*** of another block that is usable and then accessing that other block." '842 patent at 16:37-40 (emphasis added). From the plain language of the claims, it is clear that when the controller initially designates the address of an unusable non-volatile memory block as corresponding to a received host address, the controller will substitute the address of the replacement non-volatile memory

block. The controller then uses the substitute physical block address to access the replacement block for the read or write operation.

SanDisk's proposed construction is also supported by the teaching of the specification. The relevant passage states that "[w]hen the number of defective cells in a sector exceeds a predetermined number, the sector containing the defective cells is replaced by a ***substitute*** sector." '842 patent at 2:34-37 (emphasis added). This again shows that "linking" refers to substituting the physical address of an unusable block with the physical address of a block that is usable. Likewise, the preferred embodiment explains that "[w]hen the controller is given an address to access data, the controller compares this address against the sector defect map. If a match occurs then access to, the defective sector is denied and the ***substitute address*** present in the defect map is entered and the corresponding ***substitute sector*** is accessed instead. '842 patent at 11:60-65 (emphasis added). Again, "linking" refers not to building a particular map, but to substitution.

The defendants' construction is incorrect for the further reason that it excludes a preferred embodiment. In one embodiment, "a defect pointer" is stored in "a sector defect map" which resides in the defective sector itself. '842 patent at 11:44-54. The defendants' proposed construction reads-out this embodiment by requiring a table containing not only the "defect pointer"—but also "the physical addresses of unusable blocks." There is no justification for the defendants' attempt to exclude a preferred embodiment from the claims. Indeed, as the Federal Circuit has often explained that "[a] claim construction that excludes a preferred embodiment is ... rarely, if ever, correct." *Sandisk Corp. v. Memorex Prods.*, 415 F.3d 1278, 1285 (Fed. Cir. 2005).

The Court should, therefore, adopt SanDisk's proposed construction and reject the defendants' attempt to impermissibly narrow the scope of the disputed term to exclude a preferred embodiment.

d. "addresses of the individual blocks [sectors]"

SanDisk's Proposed Construction	Defendants' Proposed Construction
The term requires no construction; but if the Court does construe the term, SanDisk proposes the following: addresses associated with the individual blocks where "the individual blocks" are those blocks that store the user data and overhead information. In this context, the Court's construction for the term "sector" also applies to the term "block."	addresses of one or more defective or replacement blocks [sectors]

The disputed phrase "addresses of the individual blocks [sectors]" does not need construction. The phrase is clear on its face and construction will not enhance its clarity. Claim construction is necessary "when the meaning or scope of *technical terms and words of art* is unclear and in dispute" but "is not an obligatory exercise in redundancy." *U.S. Surgical*, 103 F.3d at 1568 (emphasis added). The dispute phrase does not meet this test.

The defendants instead seek to manufacture a non-infringement argument by completely redrafting the term "addresses of the **individual blocks [sectors]**" to mean addresses of one or more **defective or replacement blocks [sectors]**." The defendants' attempted rewrite is legally erroneous and, therefore, must be rejected.

An examination of the terms of the disputed phrase confirms that no construction is necessary. For example, the term "addresses" is not an ambiguous technical term. In apparent agreement, the defendants keep the term "addresses" in their proposed construction. So, the only remotely technical term in the disputed phrase "addresses of the individual blocks [sectors]" is "individual blocks," for some asserted claims," and "individual sectors" for others. (The parties agree that the two terms carry the same meaning.) To date, the defendants have failed to identify any ambiguity or lack of clarity with respect to the term "individual blocks." This is because the defendants cannot. The meaning of the term is clear on the face of the claim. Nevertheless, to the extent that the Court believes that ***any*** construction of this term is needed, the Court should restrict the endeavor to the term "individual blocks."

The meaning of "individual blocks" is readily apparent from its usage in the claims at issue. For instance, in claim 10 of the '842 patent, the second method step establishes the

antecedent basis for the term: "operating ***individual blocks*** of memory cells with non-overlapping portions thereof storing at least user data and overhead information." '842 patent at 17:31-33 (emphasis added). This shows that the "individual blocks" are those non-volatile memory blocks that (1) store both user data and over-head data and (2) are "operated" on by the memory system for purposes of the claimed method. '842 patent at 17:31-33 ("operating individual blocks of memory cells with non-overlapping portions thereof storing at least user data and overhead information").

Should the Court decide to construe the full term "address of the individual blocks," SanDisk's proposed construction—"addresses associated with the individual blocks"—should be adopted. The term "associated with" is a commonly understood definition for the term "of." Oxford English Dictionary at 712. This definition is also consistent with the teaching of the specification, as best illustrated by the following figure from the patent:

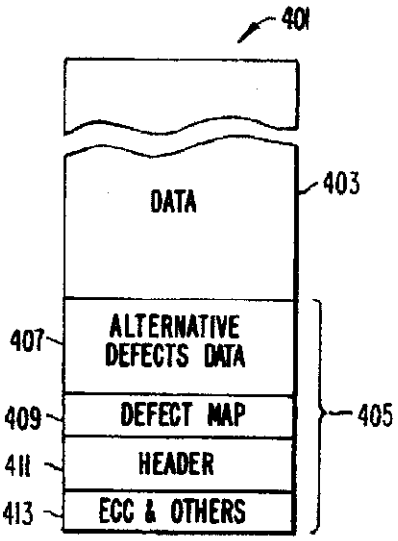

FIG. 5.

As shown above, the "header" is stored as part of the overhead data portion of a sector. The header contains the mass memory storage block address of the user data with which it is

stored. '842 patent at 9:11-16 (example of header storing the disk drive cylinder, head, sector address). This is an example of the type of "address" contemplated by the claim.

The patent explains that the controller uses this address in order to "verif[y] that the memory is accessed [*i.e.*, read by the controller] at the address that the user had specified." '842 patent at 9:17-19. Similarly, in the context of a write operation, the controller reads the header portion of the overhead data for a sector/block and uses the address information within that header to verify that it has located the correct location to write the user data. '842 patent at 10:43-50. In this example, the address is "associated with" the individual block/sector with which it is stored.

The erroneous nature of the defendants' construction of this term is clear from an examination of the patent claims. The defendants' allege that the "address of the individual blocks" refer to the "address of one or more ***defective or replacement blocks***." Neither claim 10 or 12 of the '842 patent relate to the defective or replacement blocks. There is no indication, in either of these claims, that the addresses stored in overhead are linked to the addresses of defective blocks. '842 patent at 17:20-48, 17:51-53. In contrast, dependent claim 15 recites "addresses of any defective non-volatile memory blocks." '842 patent at 18:1-6.

The inventors therefore clearly distinguished between "addresses of individual blocks" (on one hand) and "address of any defective non-volatile blocks" (on the other). The former covers addresses associated with the individual blocks while the latter pertains to the addresses associated with defective (*i.e.*, usable) blocks. To disregard this distinction is to disregard the requirement that "[w]here claims use different terms, those differences are presumed to reflect a difference in the scope of the claims." *Forest Labs., Inc., v. Abbott Labs.*, 239 F.3d 1305, 1310 (Fed. Circ. 2001).

To recap: SanDisk does not believe that construing this term is necessary. Should the Court believe that a construction would be beneficial, the Court should adopt SanDisk's proposed constructions for "individual blocks" or the full term.

e. "an address in a format designating at least one mass memory storage block" and "a mass memory storage block address"

SanDisk's Proposed Construction	Defendants' Proposed Construction
an address used by the host system to reference a block of user data in a mass storage system	an address format that includes a physical location in mass memory specified by the host system

The term "an address in a format designating at least one mass memory" appears in asserted claims 1, 10, and 61 of the '842 patent. The term "a mass memory storage block address" appears in claims 67 and 79 of the '316 patent. The parties agree that both terms carry the same meaning, but dispute what that meaning is.

First, to provide context, the parties agree that the disputed terms refer to an address used (or specified) *by the host system*. '842 patent at 17:34-40 (claim 10 recites: "causing the controller, ***in response to receipt from the host system*** of an address in a format designating at least one mass memory storage block") (emphasis added). As shown in Figure 1A of the '842 patent (reproduced above), the address from the host is sent along the "system bus" between the computer system's "microprocessor" and the memory system's controller. *See also* '842 patent at 18:23-25 (claim 20 recites: "communication of mass memory storage block addresses and user data with the controller is in parallel over a bus."). The dispute, therefore, boils down to whether the address specified by the host system *must include* a physical location.

The defendants are wrong for two reasons. First, a claim construction that excludes a preferred embodiment is "rarely, if ever, correct." *Sandisk*, 415 F.3d at 1284. Despite this unassailable authority, the defendants advocate for a construction that does just that.

In particular, the specification explains that "[i]n a normal disk system the media is divided into cylinders and sectors" ('842 patent at 7:36-38) and that "[t]he EEprom system is preferably set up to *emulate* a conventional disk" (*Id.* at 7:54-56, emphasis added). That is, the memory system looks to the host as a conventional disk. The host, therefore, provides addresses to the memory system in the same format as it would provide to a disk system. The example provided in the patent is the "Head, Cylinder and Sector" format. '842 patent at 9:12-13.

As explained in the Technology Background section, while a conventional disk drive actually has heads and cylinders divided up into sectors, flash is a semiconductor memory made of wires and transistors. Flash has neither heads nor cylinders divided into sectors. An address in the "head, cylinder, and sector" format is not a physical address for a flash memory system. Flash memory does not have any of the structure found in a disk drive. A disk drive address, in whatever format, is an address that the flash memory controller must translate into an address that the flash memory understands.

Even after translation, the controller may change the flash memory address in order to avoid defects. To do this, the '842 patent discloses "sector" remapping whereby the controller substitutes (or links) the address of a defective block with a substitute usable block. In this embodiment, the physical block (or sector) address to which the controller maps the address from the host is not constant. It could change, perhaps multiple times. There is no physical relationship between the address from the host and the location within the flash memory storing the corresponding data. Thus, to require that the address specified by the host system indicate a "physical location" is to construe the claims to exclude the preferred embodiment.

The defendants' proposed construction is wrong for a second reason: It ignores the intrinsic record of the patents (which includes the cited prior art) and the understandings of persons of ordinary skill in the art.[11] In the late 1980's when Dr. Harari and his co-inventors conceived of their inventions, it was well-understood by individuals of ordinary skill in the art that disk drives could use either "cylinder, head, sectors" addressing or logical addressing. Taylor Decl. ¶¶ 7-11. This understanding is apparent from the prosecution history of the '842 patent.

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[11] *V-Formation v. Benetton Group SpA*, 401 F.3d 1307, 1311 (Fed. Cir. 2005) ("This court has established that 'prior art cited in a patent or cited in the prosecution history of the patent constitutes intrinsic evidence."); *Kumar*, 351 F.3rd at 1368 ("When prior art that sheds light on the meaning of a term is cited by the patentee, it can have particular value as a guide to the proper construction of the term to persons skilled in the art, but also that the patentee intended to adopt that meaning.").

For example, during the prosecution of the '842 patent, the patent examiner considered the Robinson patent. The Robison patent is assigned to Seagate, one of the leading hard disk drive companies. Taylor Decl. at ¶ 9. The Robinson patent explains that, back in 1985, it was "well known in the disc drive field to convert logical block addresses into cylinder head and sector addresses as most seek commands are initially input as logical block addresses." Robinson at 3:46-49. In other words, some cited prior art to the '842 patent shows that the address sent by hosts to memory systems—*i.e.*, the "mass memory storage block address"—were typically in a logical block address format (the antithesis of a physical address) and converted into a physical address by the memory system. Given that the purpose of the '842 patent was "to emulate a conventional disk," it defies reason that the invention could be interpreted to exclude the most common addressing format at the time of the invention. '842 patent at 7:54-56.

The doctrine of claim differentiation bolsters this conclusion. For example, claim 19 specifies that the "mass memory storage block is an address of ***at least one magnetic disk block***." '842 patent at 18:20-22 (emphasis added). The Robinson patent teaches that, at the time, the SanDisk inventors filed their application, the addressing of "magnetic disks" was typically in the form of a "logical block address." It stands to reason that the disputed term must cover at least this.

In sum, the defendants' attempt to interject the term "physical" into the asserted claims should be rejected because it excludes the preferred embodiment, is unsupported by any intrinsic evidence, and is contrary to the prior art cited by the inventors. In contrast, SanDisk's proposed construction is simply a restatement of the claim language in a manner that is less terse and more understandable to the jury.

f. "an array of EEPROM cells"

SanDisk's Proposed Construction	Defendants' Proposed Construction
the memory storage elements of an EEPROM arranged in rows and columns	a contiguous group of memory storage elements arranged in rows and columns with dedicated row and column decoders

The disputed term ("an array of EEPROM cells") appears in claim 16 of the '808 patent. The parties agree that this term refers to memory storage elements arranged in rows and columns but, as explained below, disagree as to least three issues.

The first dispute pertains to the acronym "EEPROM." Even though the term expressly appears within the claim, the defendants propose that it be stricken entirely. By removing the term "EEPROM" from claim 16, the defendants violate the basic claim construction tenant that "***all claim terms are presumed to have meaning*** in a claim." *Innova/Pure Water, Inc. v. Safari Water Filtration Systems, Inc.* 381 F.3d 1111, 1119 (Fed. Cir. 2004) (emphasis added); *Ethicon Endo-Surgery, Inc. v. United States Surgical Corp.*, 93 F.3d 1572, 1582-83 (Fed. Cir. 1996) (party "invites to read [a] limitation out of the claim. This we cannot do.").

The defendants' fundamental claim construction error is magnified by the critical nature of the term "EEPROM" to the invention. The '808 patent is entitled "Flash ***EEPROM*** System." '808 patent at [54] (emphasis added). The inventors expressly distinguished their Flash EEPROM memory from other semiconductor memories, such as DRAM and SRAM, which others had tried (and ultimately failed) to use to emulate a magnetic disk. *Id.* at 1:19-24. The patent recites seven objects or goals, each of which expressly recite "Flash ***EEPROM***." *Id.* at 1:35-55 (emphasis added). The patent goes on to describe *all* preferred embodiments to include Flash EEPROM. Suffice it to say, there is no support for reading-out EEPROM from the claim language. "EEPROM" must remain where the inventors put it—in the claim.

The defendants' wholesale rewrite of the term "an array of EEPROM cells" does not stop there. They also seek to read-in two extraneous limitations found nowhere in the claims: (1) that the memory storage elements in the array be "contiguous" and (2) that the memory storage elements have "dedicated row and column decoders." Adding extraneous limitations, such as

these, is strictly proscribed by the Federal Circuit. *See Hoganan AB v. Dresser Industries, Inc.*, 9 F.3d 948, 950 (Fed. Cir. 1993) ("It is improper for a court to add 'extraneous' limitations to a claim.").

In addition to being unsupported by the intrinsic record, the defendants' proposed construction of "array" creates ambiguity, rather than provides clarity. The term "contiguous" has many different meanings and the defendants' proposed construction does not explain which meaning should apply. For example, a "contiguous group of memory storage elements" might require the individual elements (*i.e.*, the blocks) to actually be in direct physical contact with one another. Alternatively, "contiguous" might mean that the elements are merely electrically connected to one another, but not actually touching. Moreover, one dictionary defines this word both as "touching, in actual contact, next in space; meeting at a common boundary, bordering, adjoining" and as "[n]eihboring, situated in close proximity (though not in contact)." Oxford English Dictionary at 822. Which meaning do the defendants propose?

In effect, Defendants improperly asks this Court to adopt a special definition of "array" that is at odds with the understanding of persons of ordinary skill in the art. For example, by the time the SanDisk inventors applied for their patents in 1989, it was well known in the art to divide an array into physically distinct units called "sub-arrays." Taylor Decl. at ¶ 12.

At that time, several highly regarded computer companies, such as IBM, Fujitsu, Motorola, were filing patents describing an "array" divided into multiple sub-arrays. *Id.* at ¶ 13. Likewise, SanDisk's original flash memory chip consisted of an "array" divided into four physically distinct quadrants. *Id.* at ¶ 14. The memory elements of these sub-arrays in the array were not necessarily "contiguous" with one another, even though they were part of the same "array." *Id.* at ¶ 15. Further, each sub-array may have its own independent row or column decoder. *Id.* at ¶ 15.

The defendants attempt to read the term "dedicated" into the meaning of "array." But this terms also carries multiple meanings. For example, the term is defined as either "devoted to a task or purpose" and, as an alternative definition "exclusively assigned or allocated to a

particular purpose." Oxford English Dictionary at 822. Which meaning do the defendants seek to interject into the claims? And what particular purpose must these "dedicated row and columns decoders" serve? Again, the defendants' proposal fosters ambiguity and is, therefore, counterproductive.

To review, the defendants' proposed construction seeks to read-out the crucial "EEPROM" limitation while simultaneously seeking to read-in two limitations found nowhere in the intrinsic record. SanDisk's proposal avoids these clear errors and should be adopted by Court.

g. "designating a combinations of a plurality of but less than all of said multiple sectors to be erased"

SanDisk's Proposed Construction	Defendants' Proposed Construction
designating which combination of the at least two (but less than all) sectors within the EEPROM array are to be erased	setting a tag in a dedicated register for each of at least two sectors to be erased

The disputed term appears in claim 16 of the '808 patent. The parties disagree on three issues regarding this term.

First, SanDisk objects to the defendants' attempt to read-out the requirement that "less than all" of the sectors be erased together. The plain language of the claim term requires "***less than all***" of the multiple sectors to be erased. SanDisk's proposed construction stays true to this requirement while the defendants once again attempt read an express limitation out of the claim. As discussed above, it is well established that "all claim terms are presumed to have meaning in a claim." *Innova/Pure Water, Inc.*, 381 F.3d at 1119.

Not only is the defendants' position legally prohibited, it is also irreconcilable with other elements of the claim. In particular, method step (b) requires "erasing the combinations of sectors ***without erasing others of said multiple sectors***." '808 patent at 17:32-33 (emphasis added). This proves that not all of the sectors can be erased at once. Otherwise, there would be no "others of said multiple sectors" to leave un-erased.

In sharp contrast to the defendants' proposed construction, SanDisk's construction is fully consistent with (and supported by) the specification of the '808 patent, which distinguishes the invention from prior art devices. The specification states that in some "conventional Flash

erase memory devices … the entire chip is erased at one time." '808 patent at 4:33-37. The specification explains that "[t]his is very slow and requires extra memory as holding space." *Id.* at 4:41-42. The specification states that in other prior art devices "the memory is divided into blocks (or sectors) that are each separately erasable, but only one at a time." *Id.* at 4:43-46. The specification explains this second prior art approach solves the need for extra memory, the approach "still requires a time consuming sequential approach." *Id.* at 4:48-50. Therefore, the capability to designate a combination of at least two (but less than all) the sectors be erased together is, therefore, an important distinction over the prior art.

Second, SanDisk's disagrees with the defendants' attempt to read-in the limitation "setting a tag in a dedicated register" into the method step of "designating a combinations of a plurality of but less than all of said multiple sectors to be erased." The terms "setting", "tag" or "register" do not appear in claim 16 and it would be legal error to read such limitations into this method step.

The defendants' proposed construction also violates the doctrine of claim differentiation. *See Seachange*, 413 F.3d at 1368. Most notably, claim 18, which is dependent upon 16, recites "wherein designating the combination of sectors including ***setting a tag*** bit for individual ones of the sectors to be erased . . ." '808 patent at 18:8-11 (emphasis added). Likewise, claim 6 recites "a ***register associated with individual ones of the sectors to tag*** its respective sector as enabled for erasure." *Id.* at 16:38-40 (emphasis added). Had the inventors intended to limit claim 16 to setting a tag in an associated (*i.e.*, dedicated) register, they would have done so expressly. The Court should not veto the inventors' claim drafting choices, as the defendants propose.

Third, the parties dispute whether the designated sectors are located within the EEPROM array. This requirement is readily apparent from the preamble of claim 16, which recites "a memory system having an array of EEPROM cells divided into a multiple non-overlapping sectors." '808 patent at 17:25-27. From this it is clear that the "sectors" designated for erasure are within the recited array.

SanDisk's proposed construction should, therefore, be adopted by the Court.

B. The '893 Patent

The parties request that the Court construe three claim terms from the '893 patent. Following a brief overview of the relevant aspects of the '893 patent, SanDisk explains why the Court should adopt its proposed constructions.

1. Overview of the '893 Patent

On February 17, 2000, inventors Kevin Conley, Jeff Craig, and John Mangan filed the application that issued as the '893 patent. The '893 patent improved upon the technology of the '842 and '316 patents. As discussed above, one key aspect of those patents was the notion of storing overhead data and user data together in the same erase block (or sector). The inventors of the '893 patent realized that not all overhead data should be treated the same way. Some types of overhead relates specifically to the user data with which it is stored. For example, the ECC is calculated specifically to identify and help correct errors related to the storing of the data that was used to generate it. As a result, if the user data changes, so too must the ECC. Other types of overhead —such as information about the physical blocks themselves—changes rarely and had to be maintained even after an erase operation.

Armed with this realization, the inventors conceived of a flash memory system which consolidated this "physical" overhead data into blocks devoted for such overhead data. The following figure from the patent illustrates example of a system with user data blocks (on one hand) and overhead data blocks (on the other):

	UNIT 0	UNIT 1	UNIT 2	UNIT 3	UNIT 4	UNIT 5	UNIT 6	UNIT 7
	Boot Info	Boot Info.	Boot Info.	Boot Info.	Boot Info.	Boot Info.	Boot Info.	Boot Info.
	Reserved 0	Reserved 1	Reserved 2	Reserved 3	Reserved 4	Reserved 5	Reserved 6	Reserved 7
	O.H. Data 0	O.H. Data 1	O.H. Data 2	O.H. Data 3	O.H. Data 4	O.H. Data 5	O.H. Data 6	O.H. Data 7
User Data Blocks								
	Spare	Spare	Spare	Spare	Spare	Spare	Spare	Spare
	Reserved 3	Reserved 6	Reserved 7	Reserved 5	Reserved 1	Reserved 2	Reserved 4	Reserved 0

FIG._12

As shown, the overhead blocks are labeled "O.H. Data." An expanded view of the contents of a portion of an overhead block is illustrated in Figure 8 below:

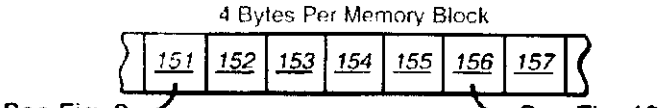

FIG._8

As shown, the overhead block includes a record of the physical characteristics for each user data block. Examples of this physical overhead included an "indication how many times the block has been programmed and erased voltage levels to be used for programming and/or erasing the block, whether the block is defective or not, and if so, and address of a substitute good block." '893 patent at 2:59-63; Taylor Decl. at ¶ 18.

Segregating physical overhead data from the user data blocks was advantageous in that it eliminated the need to read-out, and store, this physical overhead data as a precursor to each erase. '893 patent at 3:2-5. "It also reduces the amount of time necessary to access and read the block overhead data when the block is being accesses to read or write user data." '893 patent at 3:5-7.

The '893 patent also describes arranging the array of memory cells on a flash memory chip into "sub-arrays", which each constitute a physically distinct subdivision of the array, and programming a block from each sub-array together in parallel. '893 patent 2:35-43. The patent teaches that, for some embodiments, user data and ECC are programmed together while (as mentioned above) the physical overhead data are programmed into blocks designated for that purpose. '893 patent 2:44-55.

In sum, these techniques greatly enhanced the speed and durability of SanDisk's flash memory products.

2. The Disputed Claim Terms

The claims in which the disputed terms of the '893 patent appear are listed below. The disputed terms are in bold:

1. A method of operating a re-programmable non-volatile memory system having its memory cells organized into distinct blocks of simultaneously erasable cells, comprising:

designating a first group of said blocks for storing user data and a second group of said blocks for storing **information of the characteristics of said first group of blocks**,

storing, in individual ones of the first group of said blocks, user data plus characteristics of the user data being written therein but not including characteristics of said first group of blocks, and

storing, in individual ones of the second group of said blocks, a plurality of records of characteristics of individual ones of the first group of blocks but without storing either user data or characteristics of the user data into the second group of blocks.

13. The method of claim 12, wherein said at least one characteristic of the user data that is included as part of sectors of data includes redundancy codes that have been generated from user data while the user data is being transferred in a stream to said individual blocks within said first group, **individual ones of the redundancy codes being appended to ends of the user data from which they are generated** to form sectors of data.

52. A method of operating a re-programmable memory system having non-volatile memory cells organized into distinct blocks of a number of simultaneously erasable cells capable of storing a given quantity of data, the blocks of cells being further organized into a plurality of units, comprising:

receiving and temporarily storing in a buffer memory at least a given number of sectors of user data to be programmed into the memory system, **moving data in a stream from one of the given number of sectors of user data in the buffer at a time to a respective one of a given number of storage registers at a time**, and

thereafter moving the user data from the given number of storage registers in parallel to respective ones of a given number of memory cell blocks that are located within different ones of a given number of said units.

58. The method according to claim 52, wherein moving data in a stream includes generating a redundancy code from the stream of user data of the individual sectors and **appending the generated code to the ends of the user data from which they are generated**.

65. The method of any one of claims 52-57, wherein the sectors of user data stored in the memory cell blocks do not include **characteristics of the memory cell blocks in which they are stored**.

3. SanDisk's Constructions for the '893 Patent Should Be Adopted

a. "individual ones of the redundancy codes being appended to ends of the user data from which they are generated"

SanDisk's Proposed Construction	Defendants' Proposed Construction
The term requires no construction; but if the Court does construe the term, SanDisk proposes the following: each redundancy code follows the end of the user data from which it is generated with no other user data intervening	each redundancy code adjoins the end of the user data from which it is generated

The above term does not require any construction. As discussed above, the Federal Circuit has indicated that claim is necessary "when the meaning or scope of *technical terms and words of art* is unclear and in dispute" and is clear that claim construction "is not an obligatory exercise in redundancy." *U.S. Surgical Corp.*, 103 F.3d at 1568. The only technical terms of art in the element "individual ones of the redundancy codes being appended to ends of the user data from which they are generated" are "redundancy code" and "user data." But there is no dispute as to the meaning of these two terms. That is why those terms remain unchanged in both SanDisk and defendants' proposed constructions. Thus, aside from an apparent effort to wordsmith the claim, the defendant's proposal amounts to nothing more than the unnecessary substituting of the word "adjoins" for "appended."

The defendants' proposed substitution serves no legitimate purpose. It is a prohibited act of redundancy. The term "appended" is a lay term, with a readily apparent meaning. The fact finder is no more likely to understand the definition of "adjoins" than they would understand the term "appended."

Apart from being unhelpful, the defendants' proposed substitution is also legally impermissible. The defendants are attempting to conjure a non-infringement defense by rewriting the claims to include the term "adjoins" and then interpreting that term (which they added) to prohibit ***anything*** from coming between the user data and the redundancy code. The Court should reject this position and leave the plain (and easily understandable claim language) undisturbed.

SanDisk's proposed construction should be adopted to the extent that the Court decides to construe this term. It uses plain terminology—as opposed to swapping "appended" with "adjoins"—and makes sense within the context of the claims. For example, SanDisk's proposed construction makes clear that the redundancy (ECC) codes follow the end of the user data (from which it is generated) as opposed to other user data that is also programmed into the flash memory. This is best explained with reference to the following figure:

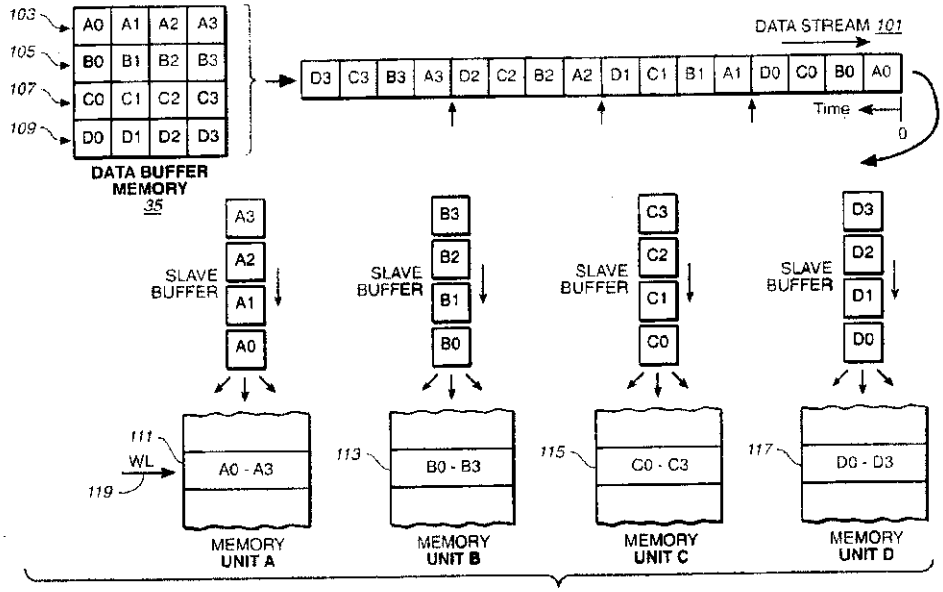

FIG._5

As shown, the user data arrives in a "datastream" from the host. The data is temporarily stored in a "slave buffer" until programmed into a block within one of the memory units. In this example, four different blocks (one from each unit) are programmed in parallel. A different redundancy code (or ECC) is generated from the data in each of these blocks. Figure 7 provides an illustration of the "manner in which data from multiple sectors is transferred to the memory array." '893 Patent at 5:8-9.

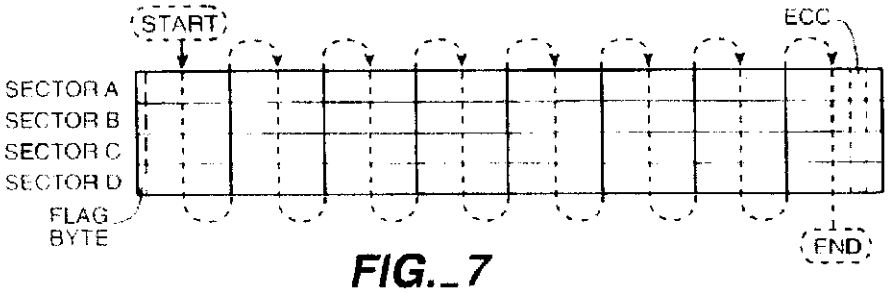

FIG._7

The figure shows that the ECC programmed into a block follows the user data from which it was generated. In other words, the ECC for a particular unit of data is stored with that data. '893 Patent at 11:66-12:6 ("After the ECC generator has received the last byte of data of a sector being stored, the final result is inserted in the last chunk of the data stream . . . . The redundancy code is then stored in the same block of the memory array as the sector of user data from which it was generated.").

The defendants' attempt to prohibit ***anything*** from coming between the user data and the redundancy code contradicts the specification. The contradiction arises because of defective columns. As shown in the following figure, the inventors provided a "spare" portion in each block to account for the possibility of defects:

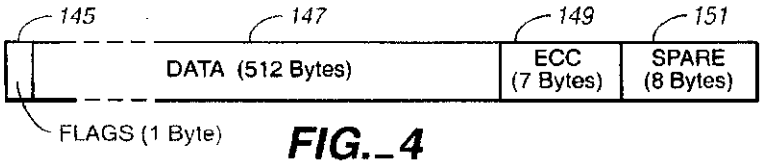

FIG._4

As shown, the exemplary block includes 512 bytes of user data, 7 bytes of ECC and 8 bytes of spare. As the inventors describe in the '893 patent, "[t]he number of spare bytes 151 will be less than what is shown in FIG. 4 by the number of fill bytes that are inserted into the user data 147 by the BCP processing 36 to avoid bad columns." '893 patent at 13:26. As illustrated in the following modified version of Figure 4, this insertion, of course, can occur anywhere including between the user data and the ECC:

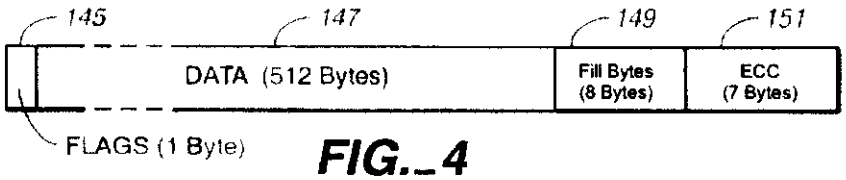

FIG._4
(Modified)

In this example, the controller interjects 8 fill bytes into that region of the block, before appending the redundancy code (ECC) at the end. In this case, all of the 8 spare bytes are used as "fill bytes" to compensate for defective memory cells in the block.

The '893 patent therefore specifically teaches that there may be intervening data between the user data and the ECC. This scenario is expressly required by claim 60, which depends upon claim 52. '893 patent at 26:12-15 ("inserting bits into the data stream for storage within cell in any defective columns, the inserted bits shifting the user data thereafter."). In other words, the defendants are once again trying to impermissibly read-out the preferred embodiment, which is "rarely, if ever, correct." *Sandisk v. Memorex Prods.*, 415 F.3d 1278, 1284 (Fed. Cir. 2005).

In summary, the disputed term does not require construction. The defendants are simply trying to swap "appending" for "adjoins" in order to foster an interpretation of the claims that is so narrow, it excludes even the preferred embodiment. To the extent that the Court does interpret the term, it should adopt SanDisk's construction, which relies on plain language terms and is consistent with the intrinsic record.

b. "information of the characteristics of said first group of blocks"

SanDisk's Proposed Construction	Defendants' Proposed Construction
physical information relating to the condition of, status of, operation of, or substitute good block address(es) of the first group of blocks	information relating to the condition of, status of, operation of, or addressing used in the first group of blocks

To a large degree, the parties agree on the proper construction for this term. There is no dispute that this term encompasses information relating to the status and operation of the first group of blocks. The dispute centers on whether the "characteristics" are physical, as SanDisk proposes, or if they could relate to ***any*** type of information, which is what the defendants'

propose. As explained below, the intrinsic evidence proves that SanDisk's construction is correct.

The first step of method claim 1 of the '893 patent involving "designating … a second group of said blocks for storing information of the characteristics of said first group of block." '893 patent at 20:20-24. The final step lends clarity by prohibiting the "second group of blocks" from "storing either user data or characteristics of user data." *Id.* at 20:29-33. Thus, the plain language of claim 1 mandates that the "characteristics of said first group of blocks" do not include characteristic information about user data. Instead, the information is related to physical attributes of the blocks themselves.

The dependent claims to claim 1 confirm that "information of the characteristics of said first group of blocks" is physical information. Claim 4 states that such characteristic information includes "programming and reading characteristics of a corresponding one of the first group of blocks." '893 patent at 20:45-46. Claim 8 states that such characteristics include "storing an indication of whether a corresponding block within said first group is defective." *Id.* at 21:9-10. Claim 9 states that such characteristics include "any of programming, reading, erase or wear characteristics of [a] corresponding block." *Id.* at 21:14-16. Claim 10 states that such characteristics include the "locations of any bad columns that extend through corresponding blocks within said first group." *Id.* at 21:20-21. Each of these dependent claims confirms that the claimed characteristic information about the first group of blocks is physical information.

The '893 patent specification also confirms that the claimed characteristic information of the first group of blocks is physical information. The relevant passages states that "the overhead information that is stored in a block along with a sector of data is limited to information about the data itself and ***does not include physical overhead information*** about the block or it operating." '893 patent at 13:61-65 (emphasis added). The patent goes on to provide examples of physical information such as "experience cycles, number of pulses or voltages required to program or erase the block of cells, defects within the block and like information about the storage media." *Id.* at 14:1-4. This information is all physical.

The defendants' proposed construction is inconsistent with the intrinsic record. Indeed, the preferred embodiment discloses storing a "flag byte" in each user data block. '893 patent at Fig. 4. This byte includes "transformation bits" which "cause the memory cells to be programmed to different states for the same data." '893 patent at 13:81-0. Under the defendants' proposal, "information relating to the condition of, status of, operation of … the first group of blocks" ***cannot be stored*** in user data blocks. Where does that leave the "flag byte"? Does that not relate to the "status" or "operation" of the first group of blocks? Thus, by refusing to accept that this information is "physical," the defendants exclude the preferred embodiment.

The defendants' proposed construction also errs in failing to specify which "addressing" information must be stored in the second group of block, but not in the first group. The '893 patent references at least ***ten different address types***.[12] By generically referencing "addresses," the defendants introduce substantial ambiguity into claim 1.

What the defendants fail to realize is that the "addresses" stored in the overhead blocks are those of the substitute physical blocks. '893 patent at 2:58-63 ("Each overhead data record may include … whether the block is defective or not, and if so, and address of a substitute good block…."); 15:20-22 ("The overhead records for these block designate their status as spares in the flag byte, and whether they are good or defective spare blocks."). The physical address of a substitute block is unrelated to the data. Taylor Decl. at ¶ 19. Other forms address information, are closely associated with the user data and, therefore, may be stored in the first group of blocks.

For example, during a write operation, a host system will provide a flash memory system with a host address and data for the write operation. Taylor Decl. at ¶ 11. The host address is tied to the data. In a subsequent read operation, when the host sends the same address, it expects

[12] The different address mentioned in the '893 patent are as follows: "address of a substitute good block" 2:62-63; "beginning address" 3:15; "logical address" 3:17; "logical block address" 4:9-10; "physical address" 4:10; "address blocks" 4:27; "byte address" 10:55; "physical memory address" 12:46; "sector address" 16:1; "physical block address" 17:58

to receive the data that was programmed into the memory during the write operation. *Id.* at ¶ 19. Because the host knows little about the physical attributes of the memory system—even whether it is a flash memory or a rotating disk drive—such an address cannot be physical.

The Court should therefore adopt SanDisk's construction and properly limit the scope of the term to "physical" information based on the intrinsic record.

c. "moving data in a stream from one of the given number of sectors of user data in the buffer at a time to a respective one of a given number of storage registers at a time"

SanDisk's Proposed Construction	Defendants' Proposed Construction
moving data in a stream from at least one of the given number of sectors of user data in the buffer at a time to a storage register at a time	moving no more than one sector of user data from the buffer to a storage register at a time

The dispute here centers on whether or not the "moving data in a stream" step restricts the memory system of claim 52 to moving one (and only one) sector of data from the buffer to the storage registers at a time. As discussed below, the intrinsic evidence for the '893 patent demonstrates that there is no such restriction.

Nothing in the claim language supports the defendants' proposed restriction "moving data in a stream" element of claim 52. The plain claim requires moving data from "one of the given number of sectors of user data in the buffer ***at a time*** to a respective one of a given number of storage registers ***at a time***." The dual usage of "at a time" indicates that while, multiple sectors may be moved from the buffer to the registers, each sector is moved into a particular number of storage registers. The claim language does not suggest that (for any given interval) the data for one, and only one, sector is moved from the buffer to their respective registers. The plain language of the claim alone dooms the defendants' proposal.

The defendants' "no more than one" limitation is further belied by the claim's use of the transitional phrase "comprising." This phrase "signals that the entire claim is presumptively open-ended." *Gillette,* 405 F.3d at 1371. For example, while the claim requires "receiving and temporarily storing in a buffer memory at least a given number of sectors of user data," nothing

prohibits this buffer from storing additional sectors on top of the "given number." Likewise, nothing in the claim prohibits additional sectors from moving from the buffer to the registers. Simply stated, nothing in the claim overcomes the presumption that the entire claim is open-ended.

Not only is the prohibition that the defendants seek to impose absent from the claim language, it is also contradicted by the specification. The relevant passage states:

> Rather than completing the transfer of chunks of data of one sector before commencing another, it is preferred to ***alternately transfer chunks of multiple sectors*** between the buffer memory 35 and different ones of the array units 0-7.

'893 patent at 9:30-33 (emphasis added). Then, in the context of Figure 5 which is reproduced above, the patent explains that these sectors are transferred in "successive bytes of a first chunk **A0** of the buffered data sector 103, followed by a first chunk **B0** of the sector **105**, then a first chunk **C0**, of the sector." *Id.* at 9:51-54. This contradicts the defendants' notion that no more than one sector is moved from the data buffer to the register.

To summarize, the "no more than one" limitation that the defendants seek to impose is unsupported by the plain language of the patent claim, belied by the claim's use of "comprising," and contradicted by the specification. The Court should, therefore, reject this absurd limitation proposed by the defendants and adopt SanDisk's proposed construction.

C. The '424 Patent

The parties request that the Court construe five terms that appear in claims 1, 3, 20 and 24 of the '424 patent. Following a brief overview of the relevant aspects of the '424 patent, SanDisk explains why the Court should adopt its proposed constructions.

1. Overview of the '424 Patent

On January 19, 2001, inventor Kevin Conley filed the application which subsequently issued as the '424 patent. The patent provides innovative algorithms for making small updates to data stored on flash memory systems (such as USB flash drives) in a fast and efficient manner.

By way of background, controllers (which, as discussed above, is the "brain" of the memory system) cannot write to individual memory storage elements on a flash chip. Rather, the controller must program an entire "page" at one time, where a "page" is typically thousands of individual memory cells. Moreover, before a controller cannot write updated data to a location in which data is already stored, the location must first be erased. The smallest chunk of flash memory data that can be erased at one time, however, is called a block, which may have over one hundred pages. As a result, changing one small piece of information requires the controller to erase an entire block, and then rewrite all of the unchanged data, as well as writing the new updated data, a slow and inefficient process. Concisely, this is the "partial-block update" problem.

Mr. Conley was not the first person to face this "partial-block update" problem. In one prior art approach (which is illustrated in Figure 4 of the '424 patent), the controller selects a new "Update Block," copies the non-updated data from the "Original block," and then write updated data into this Update Block. This approach eliminated the need for an erase operation before the update (because the Update Block was already in the erased state) but still required time-consuming copy operations to move the non-updated data from the original block to the new block.

In an alternative prior art approach (which is illustrated in Figure 6 of the '424 patent) the controller wrote the updated data into an Update Block while maintaining a partially superseded Original Block. '424 patent at 2:14-21. To keep track of which pages in the original block were superseded, the prior art controller maintained (within the original block) a flag, for each page, "to indicate they contain obsolete data." *Id.* at 2:17-18. Although this approach eliminated much of the otherwise necessary erasing and copying, Mr. Conley recognized two critical shortcomings: (1) the act of changing a flag in a superseded page had "a potential of disturbing the previously written data in adjacent pages of that same block" and (2) there is a "performance penalty of the additional program operation." '424 patent at 2:51-56.

The '424 patent offered several methods for performing partial-block updates (*i.e.*, updating fewer than all the pages in a block) without the need to update flags within the block containing the original data. In one embodiment, the controller writes original data into a page on a chip, in order, according to the logical address[13] of the original data. If the controller later receives an update for some, but not all, of the pages in a block, it writes the updated data to a different block (the "update block"). The memory system's controller distinguishes between the original block and the update block (which have a common logical address) in at least two ways.

The first of which is to store an indicator of the relative age of pages. This indicator may be stored as part of the overhead data within each page or once for each block. '424 patent at 8:57-60, 9:41-53. Then, if the host requests data for a given logical address, the controller can distinguish between the original block and update block based on this indicator. But, unlike the prior art "invalid data" flag, this indicator does not involve changing data in superseded pages.

The second approach involves "keep[ing] track of the logical offset of individual pages of data within the individual memory cell blocks, so that the updated data need not be stored with the same physical page offset as the superseded data." '424 patent at 2:58-62. "This allows more efficient use of the pages of new blocks, and even allows the updated data to be stored in any erased pages of the same block as the superseded data. *Id.* at 2:62-65.

Under either approach, the controller has a mechanism for finding the most up-to-date pages for any given block. The patent describes two ways of doing this: the "reverse-read" method and the "table" method.

The reverse-read approach involves the controller reading the pages in the reverse of the order in which they were written (most-recently written is read first, oldest is read last). '424

[13] A "physical address" refers to an actual location on a memory chip. A "logical address," by contrast, is a name associated with a piece of data wherever that data is located. For example, a person's street address is a form of physical address. A person's cell-phone number, by contrast, is a form of logical address—the cell-phone number reaches the person wherever they are physically located.

patent at 10:8-43. When the controller reads a particular logical address, it ignores any page that it later reads that also contains the same logical address. The reason being that later read (earlier programmed) pages are necessarily superseded by earlier read (later programmed) pages.

Under the table technique, the controller instead builds a table within its own internal memory in which it tracks for every logical address whether there is an updated page (and where it is) that corresponds to that address. '424 patent at 10:8-43. Although the table method consumes additional memory within the controller, it has the advantage of minimizing the number of read operations.

2. The Disputed Claim Terms

The asserted claims in which the disputed terms of the '424 patent appear are listed below. The disputed terms are in bold:

> 1. In a non-volatile memory system having a plurality of blocks of memory storage elements that are individually erasable as a unit and which are individually organized into a plurality of pages of memory storage elements that are individually programmable together, a method of substituting new data for superceded data within at least one page of one of the plurality of blocks while data in at least another page of said one block is not replaced, comprising:
>
> programming the new data into at least one page of said one or another of the plurality of blocks,
>
> **identifying the at least one page of superceded data and the at least one page of new data by a common logical address,**
>
> **recording a relative time of programming the at least one page of new data and the at least one page of superceded data**; and
>
> wherein the at least one page of superceded data is less than all the data contained in said one block.

> 3. In a non-volatile memory system having a plurality of blocks of memory storage elements that are individually erasable as a unit and which are individually organized into a plurality of pages of memory storage elements that are individually programmable together, a method of substituting new data for superceded data within at least one page of one of the plurality of blocks while data in at least another page of said one block is not replaced, comprising:
>
> programming the new data into at least one page of said one or another of the plurality of blocks,

identifying the at least one page of superceded data and the at least one page of new data by a common logical address,

recording a relative time of programming the at least one page of new data and the at least one page of superceded data; and

wherein the data in at least another page of said one block that is not replaced are not copied into said one or another block as part of substituting the new data for the superceded data.

20. In a re-programmable non-volatile memory system having a plurality of blocks of memory storage elements that are erasable together as a unit, the plurality of blocks individually being divided into a plurality of a given number of pages of memory storage elements that are programmable together, a method of operating the memory system, comprising:

programming individual ones of a first plurality of said given number of pages in each of at least a first block with original data and a logical page address associated with the original data,

thereafter **programming individual ones of a second plurality of a total number of pages less than said given number in a second block with updated data and a logical page address associated with the updated data**, wherein the logical page addresses associated with the updated data programmed into the second plurality of pages are the same as those associated with the original data programmed into the first plurality of pages, and

thereafter **reading and assembling data from the first and second plurality of pages** including, for pages having go the same logical addresses, selecting the updated data from the pages most recently programmed and omitting use of the original data from the pages earlier programmed.

24. The method of claim 20, wherein programming the second plurality of pages in a second block includes causing the updated data to be programmable in pages of the second block having different offset positions therein than the offset positions of pages within the first block containing the original data associated with the same **logical page addresses**.

3. SanDisk's Constructions for the '424 Patent Should Be Adopted

a. "recording a relative time of programming the at least one page of new data and the at least one page of superseded data"

SanDisk's Proposed Construction	Defendants' Proposed Construction
storing an indicator that allows the memory system to determine that the at least one page of new data was programmed subsequent to when the at least one page of superseded data was programmed	recording a relative time of programming = "programming into a page an indicator of the time of its programming compared to other pages written before and after that page."

This term is used in claims 1 and 3 of the '424 patent. The plain language (from both claims) supports SanDisk's construction. Claims 1 and 3 both recite a "method of substituting new data for superseded data." '424 patent at 12:64-67, 13:21-24. As part of their substitution method, claims 1 and 3 recite the step of "recording a relative time of programming the at least one page of new data and the at least one page of superseded data." *Id.* at 13:6-8, 13:30-32. In other words, whatever is recorded must indicate the relative order as between the "new data" and the "superseded data." SanDisk's construction stays true to this claim language by requiring that an "indicator" be stored which allows the controller to distinguish between the "new" data and the "superseded" data.

The specification supports SanDisk's construction. As described above, the '424 patent describes two methods of recording the relative time of programming a page: (1) writing a time stamp or counter that can be used to determine which page is the more recently programmed; or (2) "a single time stamp can be recorded for each block, either as part of the block or else where within the non-volatile memory system." '424 patent at 9:47-49. In this "block indicator" embodiment, the controller within the memory card keeps track of the relative age of the pages stored in a given block by writing them in a known order so that, within a block, the relative offset of the pages indicates when they were written. *Id.* at 9:50-53. Both embodiments involve recording a relative time of programming that allows the system to distinguish between "new data" and "superseded data," and both fall within the ordinary meaning of the claim language. SanDisk's construction is true to the ordinary meaning of the phrase, and is consistent with the

specification because it requires storing an "indicator" that allows the controller to distinguish between the "new data and the "superseded" data.

In sharp contrast to SanDisk's adherence to the intrinsic record, the defendants again seek to impermissibly read-in limitations and, in doing so (1) violate the doctrine of claim differentiation and (2) contradict the patent's specification.

For instance, the defendants seek to impose a requirement that the "relative time of programming" indicator be programmed "***into a page***." Neither claim 1 nor claim 3 recite that the "indicator" is stored in a particular location. Such limitations are only found in the dependent claims of the '424 patent. This is shown in the following table:

Defendants' Proposed Construction	Dependent Claim 7 (emphasis added)
programming into a page an indicator of the time of its programming compared to other pages written before and after that page	. . . wherein storing the value indicating a relative time of programming the new and superseded data includes ***storing individual values within the same pages as the new and superseded data which the values relate***

As illustrated in the table above, the defendants' proposed construction is substantively identical to dependent claim 7 of the '424 patent. Indeed, both require that the "indicator" is programmed / stored into each page of new and superseded data. Such a requirement is absent from the plain language of independent claims 1 and 3. By reading limitations from dependant claims into the independent claims, the defendants have again violated the doctrine of claim differentiation. *Seachange,* 413 F.3d at 1368.

The restrictions of the defendants' proposed construction would leave claims 1 and 3 so narrow as to exclude even a preferred embodiment. Such an approach is "rarely, if ever, correct." *Sandisk*, 415 F.3d at 1284. This is especially so here. As discussed above, the '424 patent discloses a "block indicator" embodiment where "a single time stamp [or indicator] can be recorded for each block...." '424 patent at 9:47-48. Under the defendants' construction, the "block indicator" would fall outside of the claims because such an indicator is not programmed into each page.

The defendants' attempt to add limitations to the claim does not end there. The language of the claim makes clear that the "relative time of programming" is between the superseded data (on one hand) and the new data (on the other hand). Yet, the defendants seek to interject a third piece of data. Namely, "other pages written … after that page." The claims never speak of pages written ***after*** the new data.

The defendants' construction is wrong for the further reason that it imports the additional limitation of requiring that the indicator distinguish a given page from "other pages written before or after that page." This limitation is completely unsupported. The claim language plainly states that the "relative time of programming" distinguishes the superseded data (on one hand) and the new data (on the other hand). There is no mention of distinguishing "other pages written … ***after*** that page." The defendants' are, nevertheless, trying to interject this requirement into the claims.

Concisely stated, SanDisk's proposed construction is in accord with the intrinsic evidence. The defendants' proposed construction, in contrast, is so overly restrictive that it violates several cannons of claim construction.

b. "logical address"

SanDisk's Proposed Construction	Defendants' Proposed Construction
"logical address" is the address provided by the host system and is distinct from the physical address of device. No further construction is needed.	"identifying the at least one page of superceded data and the at least one page of new data by a common logical address" = locating the same logical block number and logical page number within a page of superceded data and a page of new data."

The parties disagree as to whether the entirety of the following phrase requires a construction: "identifying the at least one page of superseded data and the at least one page of new data by a common logical address." Aside from the term "logical address," all the other words in the quoted phrase have a well-accepted meaning in the English language and are, therefore, readily understandable to the ultimate finder of fact. As for the term "logical address," the parties' constructions differ considerably.

SanDisk submits: (1) that the term "logical address" refers to an address provided by the host system; and (2) that the logical address is distinct from the physical address of the device. This construction is consistent with the ordinary meaning of the term, and its usage in the patent specification. For example, the '424 patent explains that a "logical address" is an address that a memory system receives from a host (such as a computer). '424 patent at 5:46-49 ("The controller **301** receives a command from the host … at a particular logical address.").

The patent goes on to explain that the "logical address" received from host computer is distinct from a physical address. For example, at column 1, lines 51-57, the patent states that a memory system controller performs the function of "translation between logical addresses (LBAs) received . . . from a host, and physical block numbers (PBNs) and page addresses within the memory cell array." '424 patent at 1:51-57. This translation is further illustrated in Figure 12 of the '424 patent, which provides a table "showing the correspondence between logical data and physical page addresses." *Id.* at 10:44-46.

The distinction between "logical address" and "physical address" is further confirmed by the claims. Both claims 1 and 3 use a "common logical address" to identify both superseded data and new data. In other words, a logical address identifies "data" as opposed to a particular location within the flash. Claim 10, which depends on claim 1, recites "building a table in volatile memory including multiple physical block addresses for the common logical address." '424 patent at 13:63-65. From the claim language alone, it is clear that a "physical address" and a "logical address" are distinct from one another. This conclusion is supported by the specification, which repeatedly distinguishes between logical and physical addresses.[14]

[14] The extrinsic evidence also supports SanDisk's construction. Technical dictionaries and definitions support the distinction between logical and physical addresses. *See* Smith Decl. Ex. 15 (IEEE Dictionary defines "logical" as "[p]ertaining to a view or description of data that does not depend on . . . physical storage" or "[p]ertaining to the form of data organization, hardware or system that is processed by an application program; it may be different from the real (physical) form. Contrast: physical"); *see also* Smith Decl. Ex. 14 (Webster's Dictionary defining address as "11: a location (as in the memory of a computer) where particular information is stored; also: the symbols (as digits or letters) that identify such a location").

The defendants' proposed construction improperly seeks to restrict the meaning of "logical address" to "logical block number and logical page number." Such a restriction is at odds with the specification, which confirms that the term "logical address" covers the addresses (LBAs) received from the host. Specifically, the specification states:

> The subsystem controller in a large block system performs a number of functions including the translation between ***logical addresses*** (LBAs) received by the memory sub-system from a host, and physical block numbers (PBNs) and page addresses within the memory cell array. This translation often involves use of ***intermediate terms for a logical block number (LBN) and logical page.***

'424 patent at 1:59-63 (emphasis added). As shown in the above passage, the terms "logical block number" and "logical page" are used in connection with the process of converting the "logical address" into a physical address. From this passage, it is clear that a "logical address" is not the same thing as a logical block number and logical page. At most, the combination logical block number and logical page is a *type* of logical address or perhaps a *portion* of the logical address. Thus, by attempting to define "logical address" as the combination of "logical block number and logical page number," the defendants contradict the specification, which treats the terms as having different meanings.

The defendants' proposed construction is wrong for another reason. It requires that the "logical address" be identified "within a page." In other words, it presupposes that the logical address was programmed into the pages of flash memory. Unlike numerous other claims of the '424 patent, claims 1 and 3 say nothing about programming a logical address into a page. Compare claim 3 ("programming the new data into at least one page) with claim 20 ("programming … updated data and a logical page address associated with the updated data"). Thus, had the inventor wished to limit claims 1 and 3 circumstances where some sort of logical address was programmed into the page with the user data, he would have done so expressly like he did with respect to other claims in the patent.

Claim 9, which depends upon claim 1, and requires "recording at least part of the common logical address in the individual pages as overhead data." '424 patent at 13:60-62. Claim 1 cannot, therefore, require that the ***entire*** common logical address be programmed into the pages. That would render a defendant claim ***broader*** than the independent claim upon which it relies and would violate the principle of claim differentiation. *Phillips*, 415 F.3d at 1315 ("the presence of a dependent claim that adds a particular limitation gives rise to a presumption that the limitation in question is not present in the independent claim.")

Accordingly, the phrase "logical address" should be construed to mean "address provided by the host system and is distinct from the physical address of device.

c. "programming individual ones of a first plurality of said given number of pages in each of at least a first block with original data and a logical page address associated with the original data"

SanDisk's Proposed Construction	Defendants' Proposed Construction
writing pages in a group of one or more blocks with original data and an ***logical address that identifies a logical location of the pages*** containing the original data	writing pages in a first group of blocks with original data and ***an address consisting of a logical block number and a logical page offset that identifies the logical location of a page*** containing the original data

The parties' dispute regarding this portion of claim 20 boils down to the meaning of the phase "logical page address." Since that is the issue, the parties' respective construction of that portion of the overall phase is bolded and italicized. As explained below, SanDisk's proposed construction is based on a proper interpretation of the intrinsic evidence while, in contrast, the defendants try to improperly read-in one particular embodiment, to the exclusion of other embodiments.

From the language of the claim, it is evident that a "logical page address" is (1) a type of logical address (2) is associated with particular pages of either "original data" or "updated data" and (3) is programmed into a page of a block with the aforementioned data. The last step of claim 20 itself uses the term "logical address" when it speaks of original and updated "pages having the same logical address." '424 patent at 15:33-34. A "logical page address," then, is a

logical address that identifies the logical location of the pages containing the associated data (*i.e.*, either original or updated data).

The term "logical page" appears throughout the specification. Understanding the meaning of this term is instructive because, quite literally, a "logical page address" is an address of a logical page. For example, the specification states that "[t]he order of ***the logical pages within*** a logical block is fixed with respect to the corresponding physical pages within a physical block." '424 patent at 5:52-54 (emphasis added). From this, it is clear that "logical page" refers to a particular page(s) within the "logical block," which is a larger unit. Hence, a "logical page address" is a logical address for ***pages*** as opposed to a logical address for the entire block.

The patent goes on to explain the benefits of a logical page address over other less granular forms of logical address: "By keeping track of the individual ***logical page*** numbers, the updated data need not necessarily be stored in the same page offset of the new block as that of the old block where superceded data is contained." '424 patent at 9:1-7 (emphasis added). An example is illustrated in the following figure from the patent:

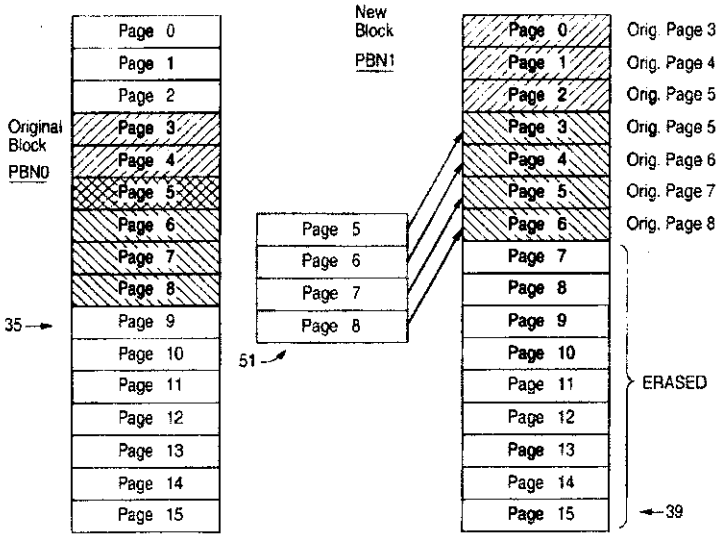

FIG. 11

The figure shows that by using an address of a logical page (as opposed to some other form of logical address) updated data stored in the "New Block" need not be stored at the same

physical offset as their now superseded counterparts in the "Original Block." In this example "the data of ***logical page*** 5 is being updated for a second time." '424 patent at 10:13-14 (emphasis added). As shown, the original version of the data associated with logical page 5 is located in page 5 of the Original Block. An initial updated version of that logical page is stored in physical page 2 of the New Block. Another version of logical page 5 is then stored at physical page 3. This reinforces that a "logical page" refers to a particular page(s) within the "logical block" (in this case pages 0 through 15 collectively). By extension, a "logical page address" refers to a logical address identifying a particular logical page among other logical pages.

Defendants, by contrast, seek to limit the phrase to a narrow, particular way in which a logical page address could be constructed. In particular, they assert that "logical page address" refers solely to "an address consisting of a logical block number and a logical page address."

The defendants' assertion is wrong because they impermissible limit the claim to a preferred embodiment. *Phillips*, 415 F.3d at 1323 (expressly "reject[ing] the contention that if a patent describes only a single embodiment, the claims of the patent must be construed as limited to that embodiment"); *Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1326 (Fed. Cir. 2002) (rejecting a proposed rule that "where only one **embodiment** is disclosed in the specification, claim terms are limited to the **embodiment** disclosed"). Where the patent expressly discloses multiple embodiments—as is the case here—the error in limiting the claim language to cover only one of them is even more obvious.

According to the patent, the non-volatile memory system receives a logical address from a host computer that is translated by the memory controller into a physical address in the memory array. '424 patent at 1:51-55. This "translation often involves the use of intermediate terms for a logical block number (LBN) and a logical page." *Id.* at 1:51–57. In this example, a logical page is *distinct* from logical block number. Thus, contrary to the defendants' assertion, the patent does not define a logical page to necessarily include a logical block number.

The description of the embodiments in the patent gives examples of at least four other variations of logical page addresses: ***1.*** "LBN and a page offset" (*Id.* at 8:12-13); ***2.*** "LBA and

page offset" (*Id.* at 8:60); ***3.*** "LBN and page tag" which is a logical page offset (*Id.* at 9:29-30); and ***4.*** "LBN and page number" (*Id.* at 9:44-45). It follows, therefore, that while a "logical page address" could include both a logical block number and logical page offset, having this particular format is not absolutely necessary. Other variations are possible and, indeed, suggested by the specification.

In sum, the intrinsic record proves that SanDisk's proposed construction of "logical page address" is correct. It is a logical address that identifies the logical location of the pages containing the associated data (*i.e.*, either original or updated data). The defendants' proposed construction is a transparent attempt to impermissibly restrict claim 20 of the '424 patent to a particular embodiment, to the exclusion of others. The Court should, therefore adopt SanDisk's proposal.

d. "programming individual ones of a second plurality of a total number of pages less than said given number in a second block with updated data and a logical page address associated with the updated data"

SanDisk's Proposed Construction	Defendants' Proposed Construction
writing fewer than all of the pages in a second block with updated data and a logical page address, but without marking the original (now superseded) pages of data in the first block with an invalid data flag	writing fewer than all of the pages in a second block with updated data and an address consisting of a logical block number and a logical page offset that identifies the logical location of a page containing the updated data

There are two disputes as to the construction of this term: (1) the meaning of "logical page address" and (2) whether SanDisk disclaimed marking superseded pages of data in the first block with an invalid data flag. With respect to the former, SanDisk proposed construction retains the claim term "logical page address" since that term's meaning is addressed in the context of the prior element.

Regarding the second issue, the intrinsic record demonstrates that this prior art technique was clearly and unambiguously disavowed.

Turning to the second issue it is well established that disavowing actions or statements made in prosecution that are "both clear and unmistakable," cause prosecution disclaimer to

attach. *Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1326 (Fed. Circ. 2003). That is the case here.

To be specific, during prosecution SanDisk added what eventually issued as claim 20 of the '424 patent. In connection with that submission, SanDisk made the following representation:

> As explained in the text of the present application, this method of updating a number of pages of data less than a full block avoids having to move unchanged pages of data from the original block to the new block in which the updated pages are written. This also frees the operation from a constraint of having to store data in the new block in pages with the same offset as the original block, a feature specifically recited in dependent claims 28 and 30. ***The need to mark the original pages of data with an invalid data flag, with its potential of causing data disturbs is also avoided.*** The technique manages operation of large blocks of stored data in an efficient manner.

March 26, 2003 Prosecution History at 6 (emphasis added). On April 28, 2003, the patent examiner allowed claim 20 in light of this statement. The emphasized portion of this statement makes clear that (unlike the prior art described in the body of the '424 patent) the update process did not involve marking a flag in the superseded pages of the original block.

The above disclaimer is consistent with the specification, which identifies the avoidance of "flags" was one of the main goals of the invention. For example, after describing the prior art systems, the '424 patent explains the problem it sought to solve:

> What is needed is a mechanism by which data that partially supercedes data stored in an existing block can be written ***without*** either copying unchanged data from the existing block or ***programming flags to pages that have been previously programmed.***

'424 patent at 7:8-12 (emphasis added).

The above term should, therefore, be construed to reflect the disclaimer. To this end, SanDisk's proposed construction tracks the language of the prosecution history and therefore accurately conveys the scope of the disclaimer. The Court should accept SanDisk's proposal.

e. "reading and assembling data from the first and second plurality of pages"

SanDisk's Proposed Construction	Defendants' Proposed Construction
reading data from the first and second plurality of pages and organizing such data by associated logical addresses	reading the logical page address within the first and second plurality of pages and thereafter assembling the data portions from the most up-to-date pages into a data file

The intrinsic evidence makes clear that "reading" and "assembling" refer to distinct operations. As discussed below, SanDisk's proposed construe correctly delineates between these operations and proposes the correct construction for each.

i. The proper interpretation of "reading"

The term "reading" refers to reading the data from the first and second plurality of pages. '424 patent at 10:60 - 67. This is evident from the plain language of the claim which states that it is the ***data*** that must be read from the first and second plurality of pages.

The patent discloses at least two embodiments for reading: the reverse read method and the table method. The reverse read method enables a controller to distinguish new data (stored in an update block) from old data (stored in an original block) by reading the pages of memory in the two blocks in the reverse of the order in which they were programmed. '424 patent at 9:54-10:43. Reading the pages in reverse order means that the controller will read the more recently programmed pages before it reads the older pages. Thus, once the controller reads a page with a particular logical address, it knows it is free to skip or ignore any later page which has the same logical address, as the later-encountered page will necessarily contain data that has been superseded by the updated data in the earlier-read page having the same logical address.

The "table" method that can be used "when the reverse page reading technique is not used." '424 patent 10:43-59. In the table method, the controller maintains a table in a separate RAM portion of the controller memory (RAM is a type of memory that, unlike Flash memory, is easily updated) that maps the correspondence between a given logical address and the physical address in the memory where the associated data is stored. The following figure provides an example of this table:

LBN	Page	PBN0	Page	PBN1	Page
0	0	0	0		
0	1	0	1		
0	2	0	2		
0	3	0	3	1	0
0	4	0	4	1	1
0	5	0	5	1	3
0	6	0	6	1	4
0	7	0	7	1	5
0	8	0	8	1	6
0	9	0	9		
:	:	:	:	:	

FIG. 12

Under the table method, when the host provides the controller with a particular logical address, the controller checks the table to see whether that logical address is associated with an update block (the third column) or only an original block (the second column). If there is an update-block entry, then the controller will select the updated page and omit the original page. For example, in response to a logical address with LBN=0 and Page=3, the controller first inspects the third column and find an entry for physical block number ("PBN") = 1 and Page =0. This physical address entry represents the up-to-date location of the data corresponding to the logical address. By way of another example, in response to a logical address with LBN=0 and Page=1, the controller again first looks into the third column. There is no entry because the data associated with that logical address has not been updated. Armed with this knowledge, the controller inspects the second column. There, the controller find an entry for PBN=0 and Page 1 which is the physical address of the data. As this description suggests, under the table method, the controller does not necessarily read logical page address information from the pages ***at all***. Rather, it relies on the logical page address information ***in the table*** during the reading and assembling step.

The defendants' construction is wrong because they attempt to strike the term "reading the data" and replacing it with "reading the logical page address." The defendants seemingly forget that claim construction entails "look[ing] to the words of the claims themselves ... to

define the scope of the patented invention." *Vitronics*, 90 F.3d at 1582. Claim 20 is very clear that "data" is one thing while a "logical address" is something quite different. To conflate the two, or otherwise suggest that one could mean that other, flies in the face of the intrinsic record and basic principles of claim construction.

ii. The proper interpretation of "assembling"

The term "assembling" refers to organizing the read data by its associated logical addresses such that the most recently programmed data is assembled in the proper order. *See* '424 patent at 15:59-60. This is exemplified in Figure 13 of the patent:

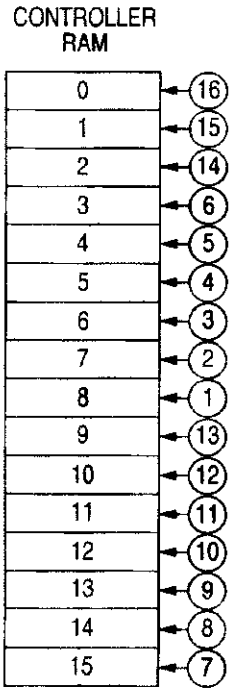

FIG. 13

As shown, during this read operation, the data is assembled in proper logical address order in the controller RAM of Figure 13. The ordering of this data is shown by the circle number of Figure 13. For example, the data read from page 6 of update block PBN1 shares the same logical address as page 8 of the original block (and the original logical block as illustrated by Figure 12). When the data from page 6 of the update block is read, it is placed in the logical location associated with the data that was originally stored in page 8 of the original block.

As a result, when the assembling operation is complete, the data in the controller RAM has the same logical order as the original data written into original block PBN0 and, thus, can be sent to the host computer system in expected logical (LBA) order. *See* '424 patent at 7:51 - 53 (data written into blocks in the same order as "the low order bits of its logical address (LBA)").

Thus, from the intrinsic record, it is clear that "assembling" refers to organizing such data by associated logical addresses.

The defendants do not attempt to construe "assembling data," even though that is the key technical terms for which a construction is needed. Instead, the defendants seek to add terms from the specification in order to impermissibly narrow the scope of the claims. In fact, *every very single word* that appear in this claim terms, finds its way into the defendants' proposed construction, except, of course, each word is now surrounded by several other words.

For example, the defendants have somehow concluded that "assembling data" requires the pages to be assembled into a "data file." To the contrary, there is nothing in the claim language that requires that the assembled data be placed in a "data file." Certainly, the phrase "data file" appears nowhere in claim 20.

In sum, the correct construction of "reading and assembling data from the first and second plurality of pages" is "reading data from the first and second plurality of pages and organizing such data by associated logical addresses."

V. CONCLUSION

For the foregoing reasons, SanDisk respectfully requests the Court to construe the identified language of the '842, '316, '808, '893 and '424 patents based on SanDisk's proposed construction.

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RESPECTFULLY SUBMITTED,

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